

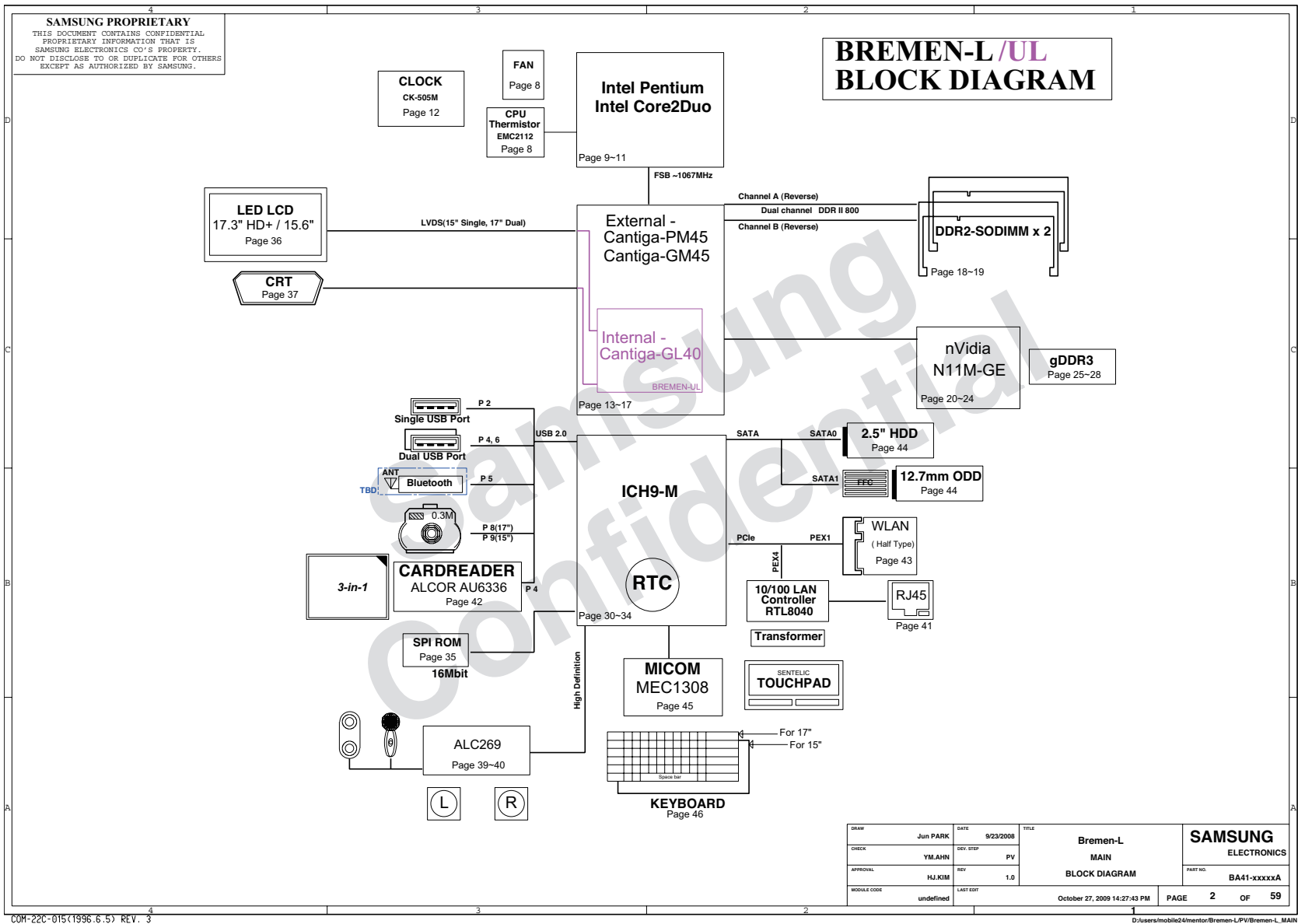
8. Block Diagram and Schematic

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<h1>Bremen-L</h1>																							
CPU : Intel Penryn																							
Chip Set : Intel Cantiga & ICH9M																							
Remarks : Montevina Platform																							
<div>Model Name : Bremen-L</div> <div>PBA Name : MAIN</div> <div>PCB Code : GCE : NAN : HAN :</div> <div>Dev. Step : PV</div> <div>Revision : 1.0</div> <div>T.R. Date : 2009.10.27</div>																							
<table border="1"><thead><tr><th>Design</th><th>CHECK</th><th>APPROVAL</th></tr></thead><tbody><tr><td> </td><td> </td><td> </td></tr><tr><td> </td><td> </td><td> </td></tr></tbody></table>				Design	CHECK	APPROVAL																	
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Owner : SEC Mobile R & D Signature : X																							
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COM-220-015(1996.6.5) REV. 3

D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

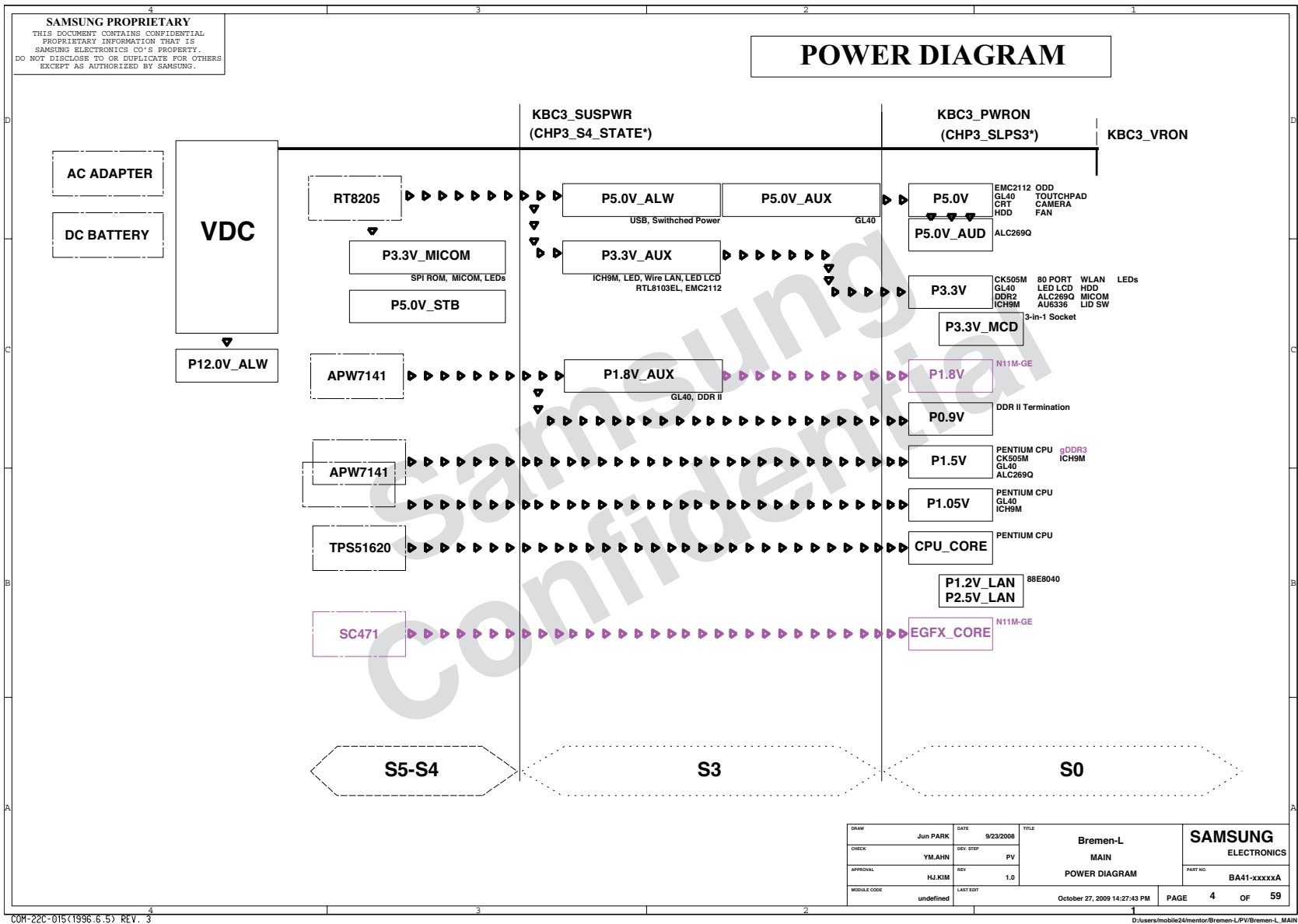
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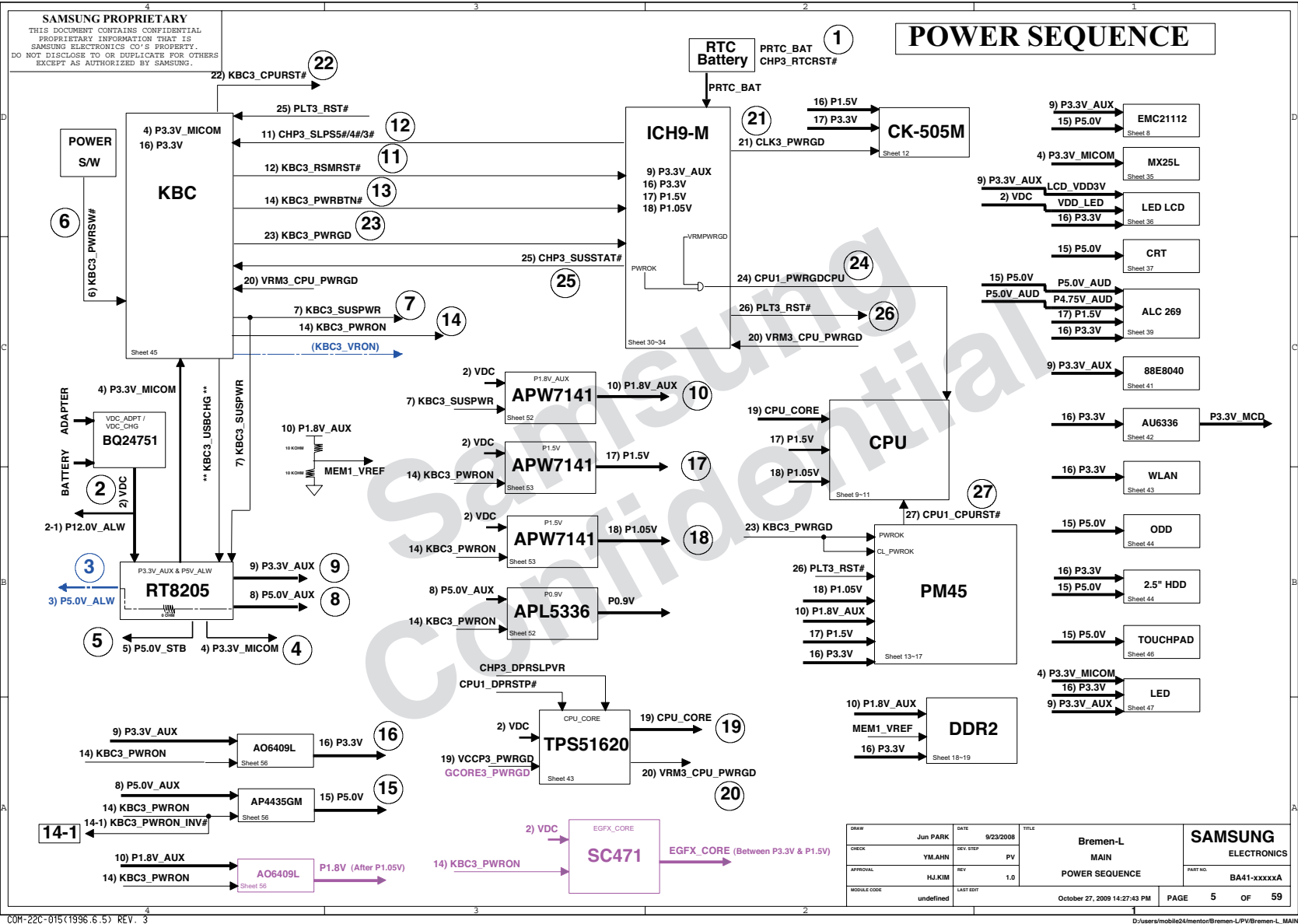
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION			
I ² C / SMB Address			
Devices	Address	Hex	Bus
ICH9M	Master		SMBUS Master
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	
SODIMM1	1010 001X	A4h	
MICOM	Master		
BATTERY EMC2102	0001 011X	16h	
	0111 101X	7Ah	
USB PORT Assignment			
Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCL_0	0 USB PORT (RIGHT, SUB)	UHCL_3	6 USB PORT (RIGHT, SUB)
UHCL_1	2 USB PORT (LEFT)	UHCL_4	8 CAMERA(17")
UHCL_2	4 CARD READER(AU6336)	UHCL_5	10 CAMERA(15")
	5 BLUETOOTH(TBD)		11
SATA Assignment			
Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
SATA0	HDD	SATA1	ODD
SATA2	-	SATA3	-
PCI EXPRESS Assignment			
Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
PCle1	WLAN	PCle2	Wired LAN
PCle3	-	PCle4	-
Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	
Crystal	10MHz	MICOM	
Crystal	14.318MHz	CLOCK-Generator	
Crystal	25MHz	LAN	
Voltage Rails			
Power Rail	Descriptions	Power Rail	Descriptions
VDC_ADPT	Primary DC system power supply (9 to 19V)	P1.05V_PEG	P1.05V (Direct Media Interface Compensation)
VDC	Charger Reference Voltage Source	P5.0V	5.0V Power Rail (off in S3-S5)
VDC_CHG	3.3V supply for the RTC well.	P3.3V	3.3V Power Rail (off in S3-S5)
PRTC_BAT	5.0V always power well	P1.05	1.05V Power Rail (off in S3-S5)
P3.0V_ALW	12.0V always power well	P0.9V	DORC Termination
P12.0V_ALW	Power Chip Reference	P5.0V_AUX	5.0V Power Rail (off in S4-S5)
P1.7V_VREF	Power Chip Reference	P3.3V_AUX	3.3V Power Rail (off in S4-S5)
P2.0V_VREF	Power Chip Reference	P1.8_AUX	1.8V Power Rail (off in S4-S5)
P5.0V_VREF_FILT	Power Chip Reference	CPU_CORE	Core Voltage for CPU
P3.3V_MICOM	Output voltage of RT8205AGQW (if VDC is removed, it will be off)	AUD_P5V	5.0V supply for Audio
LCD_VDD3V	3.3V (LED LCD)	P4.75V_AUD	Audio Analog Voltage
KBC3_CHG4.2V	To charge battery	P5.0V_STB	To charge USB device at sleep status
P1.2V_LAN	Internal Regulator's Power of LAN Controller	P5.0V_ODD	5.0V supply at SUB_ODD Board
P2.5V_LAN	3.3V (3-in-1 Socket)	EGFK_CORE	nVidia Graphic Chip power
P3.3V_MCD		P1.5V	1.5V Power Rail (off in S3-S5)
		P1.5_AUX	1.5V Power Rail (off in S4-S5)
		P1.8V	1.8V Power Rail (off in S3-S5)
REVISION HISTORY			
See rev notes for more information.			
<div> <div>4</div> <div>3</div> <div>2</div> <div>1</div> </div> <div> <div> <div> <div>DRAW Jun PARK</div> <div>CHECK YMLAHN</div> <div>APPROVAL HJ.KIM</div> <div>MODULE CODE undefined</div> </div> <div> <div>DATE 9/23/2008</div> <div>DEV STEP PV</div> <div>REV 1.0</div> <div>LAST EDIT</div> </div> <div> <div>TITLE Bremen-L MAIN BOARD INFO</div> <div>October 27, 2009 14:27:43 PM</div> </div> <div> <div>SAMSUNG ELECTRONICS</div> <div>BA41-xxxxxA</div> </div> <div> <div>PAGE 3</div> <div>OF 59</div> </div> </div> </div>			

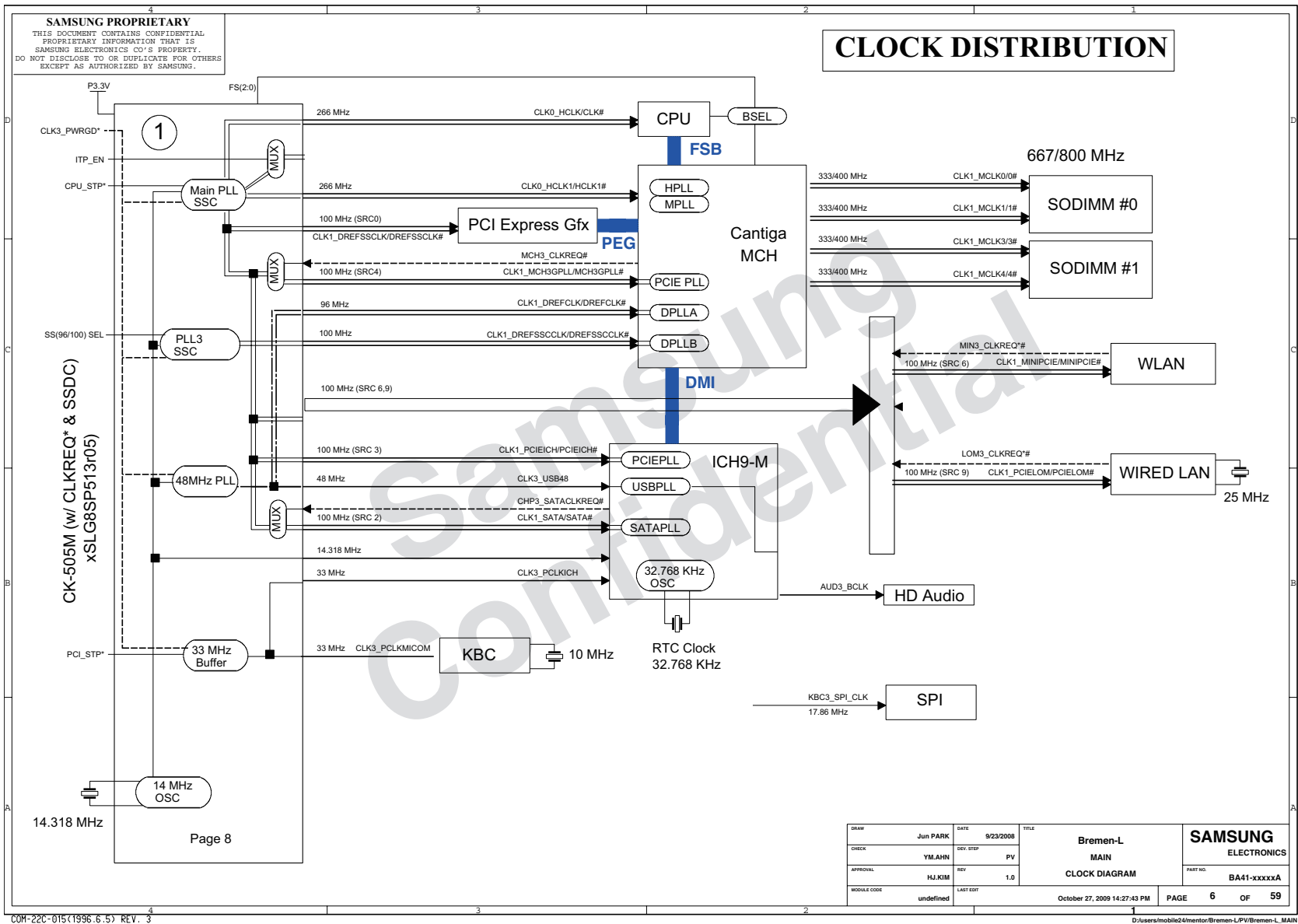
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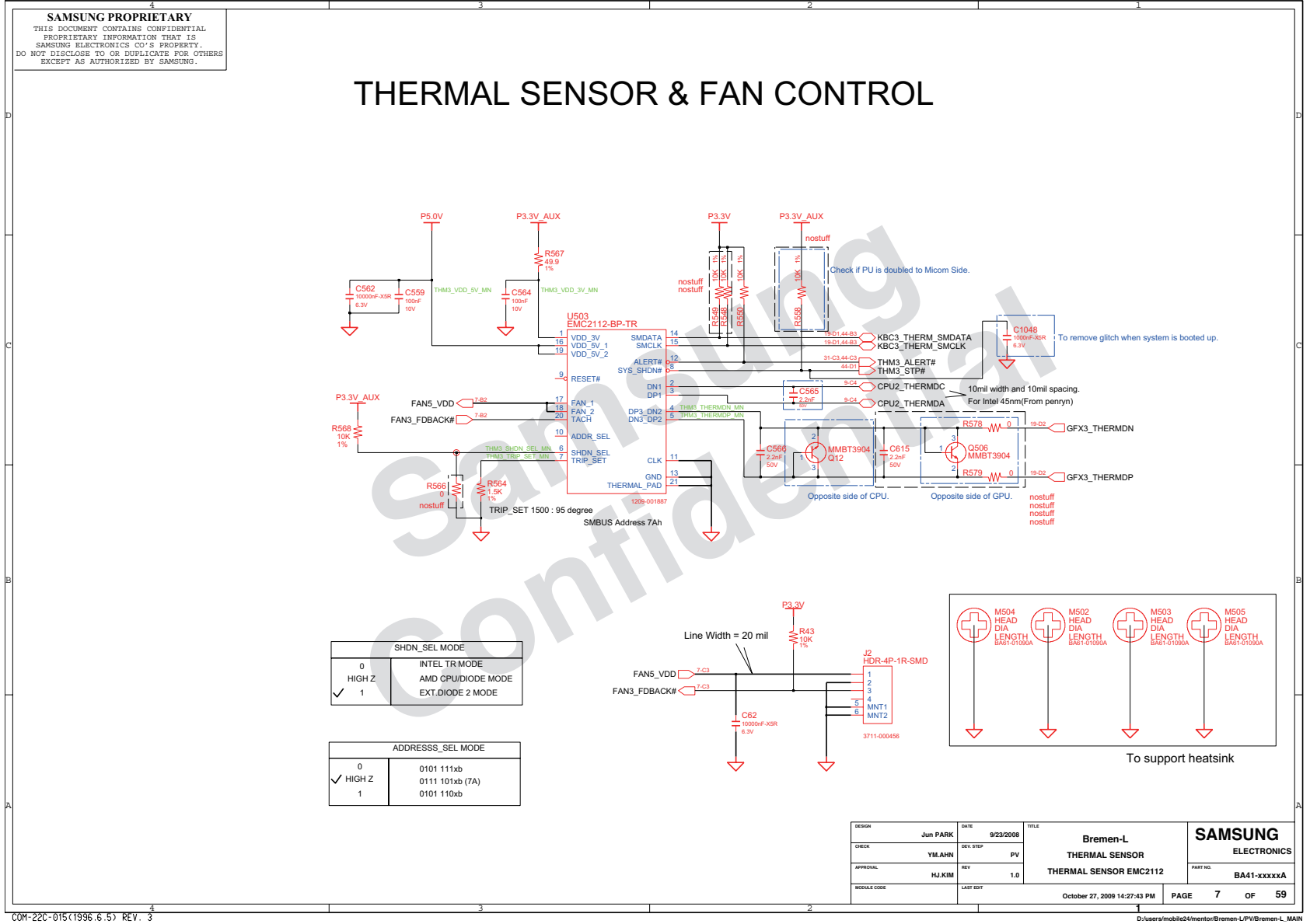
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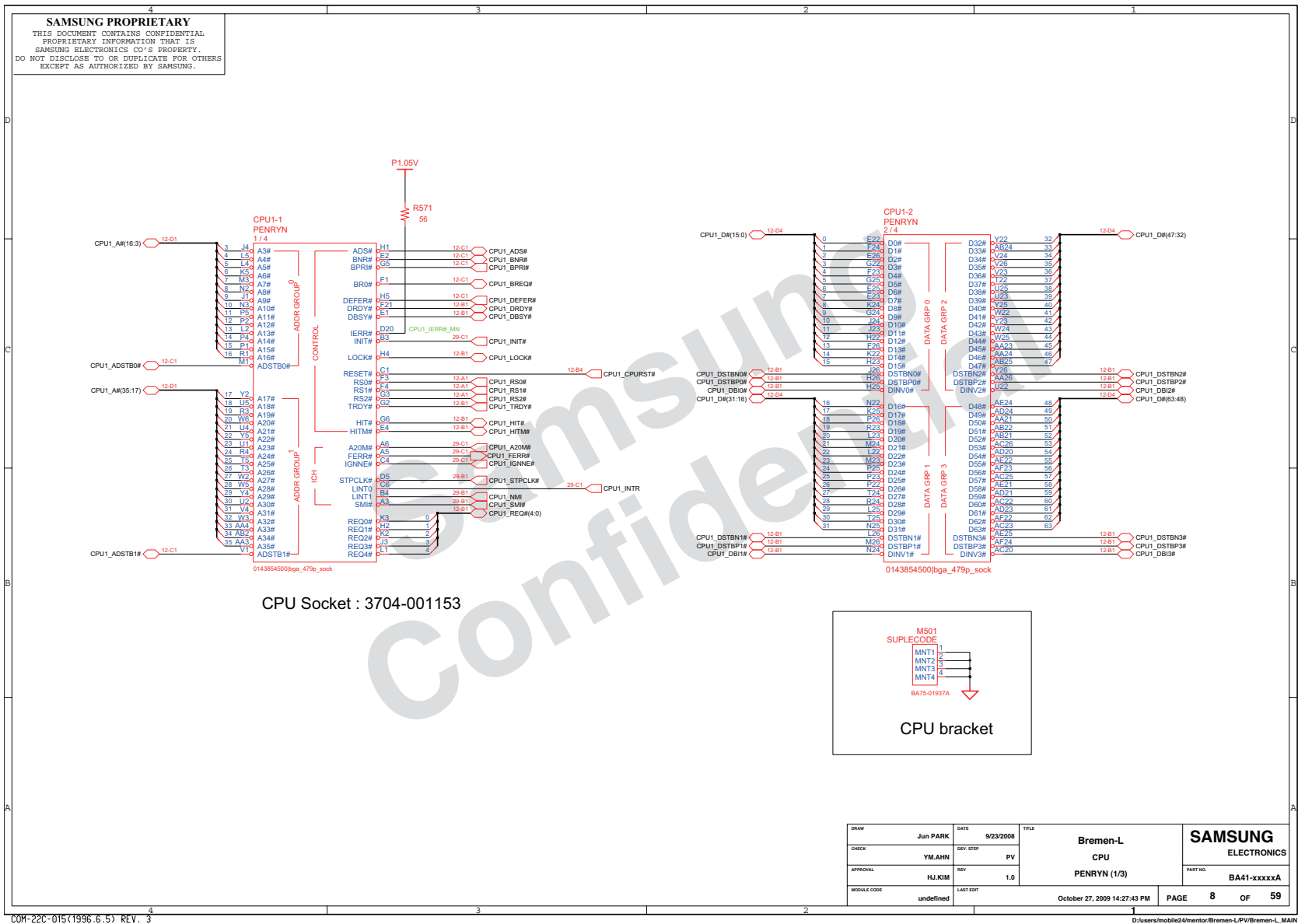
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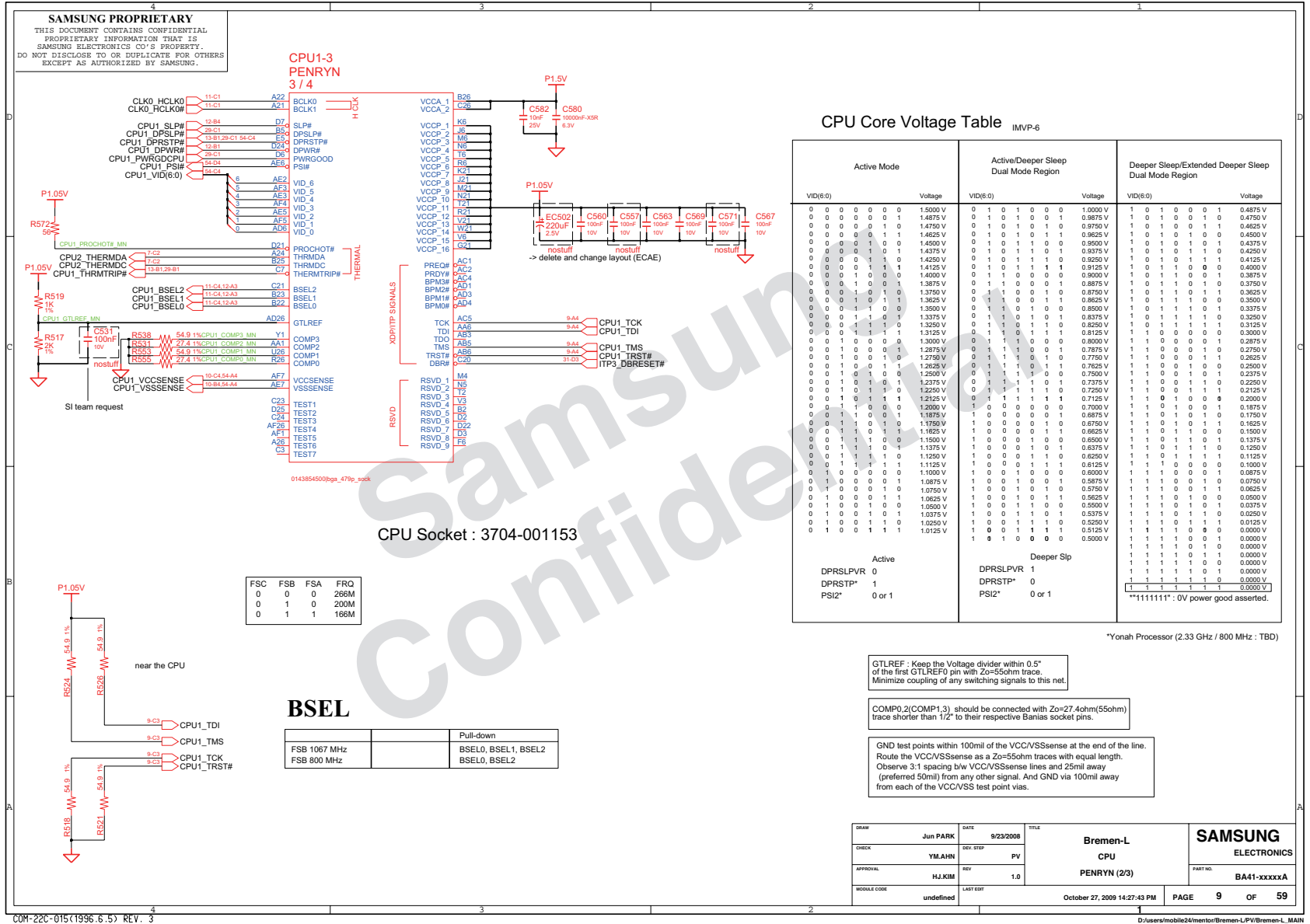
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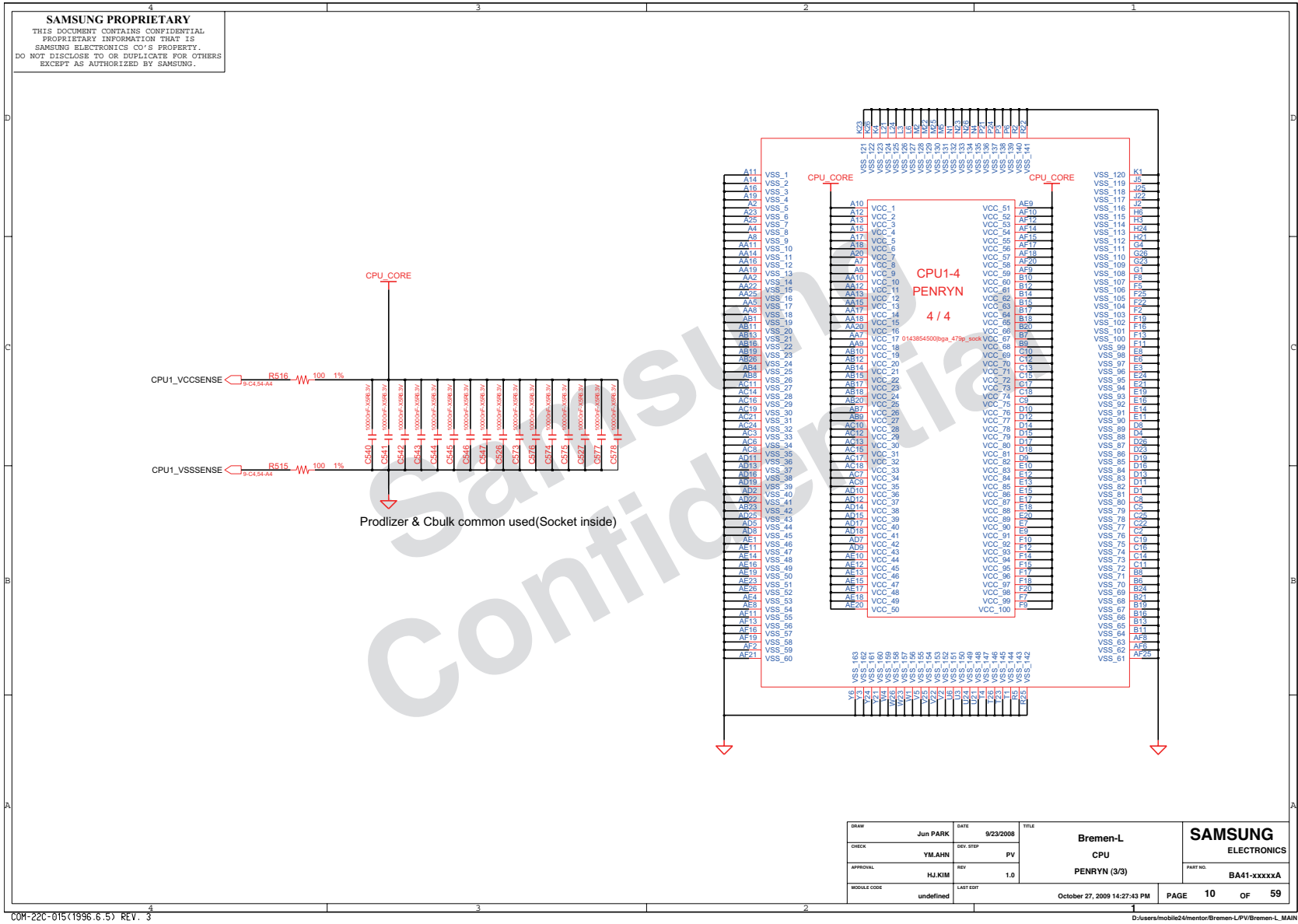
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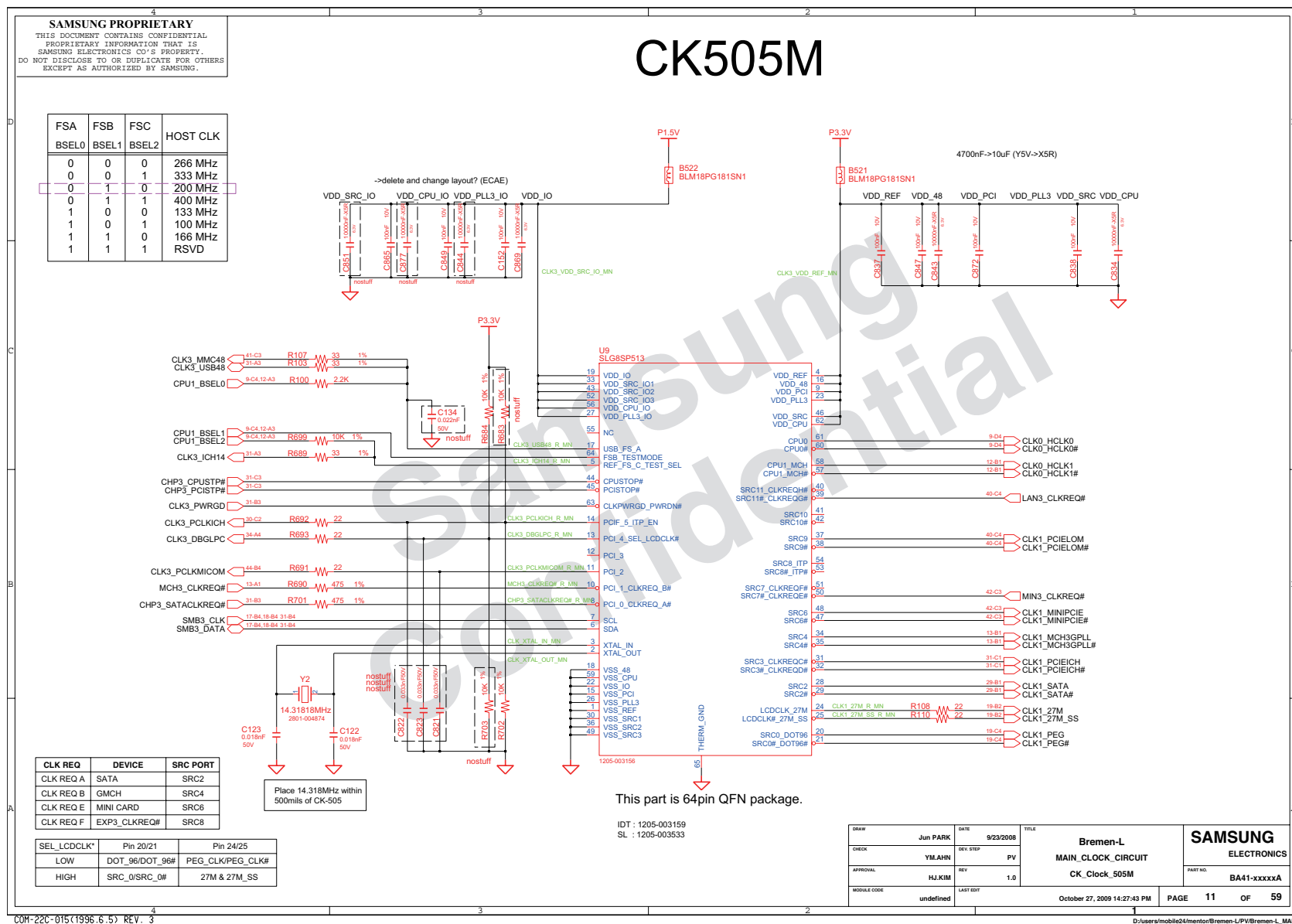
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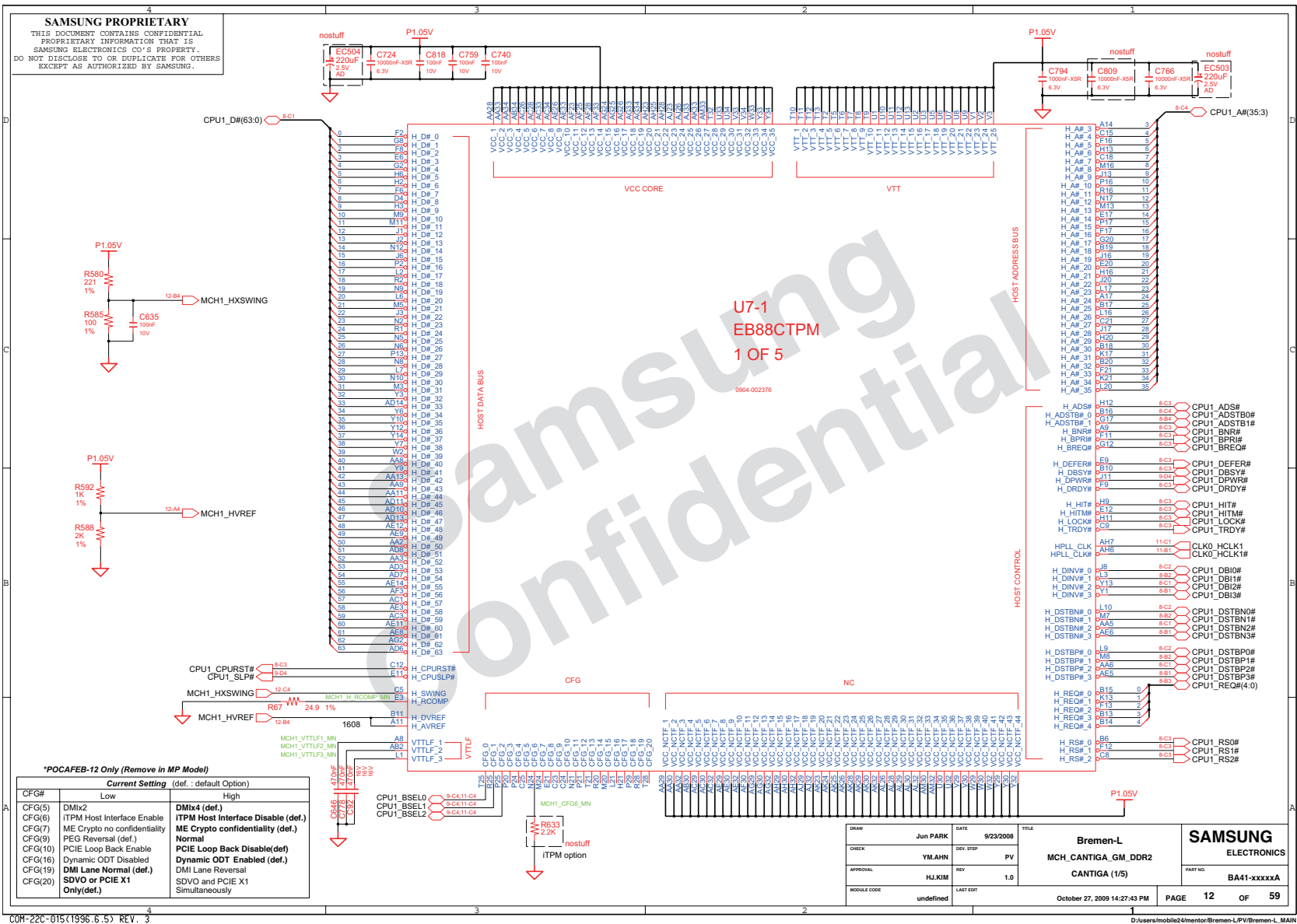
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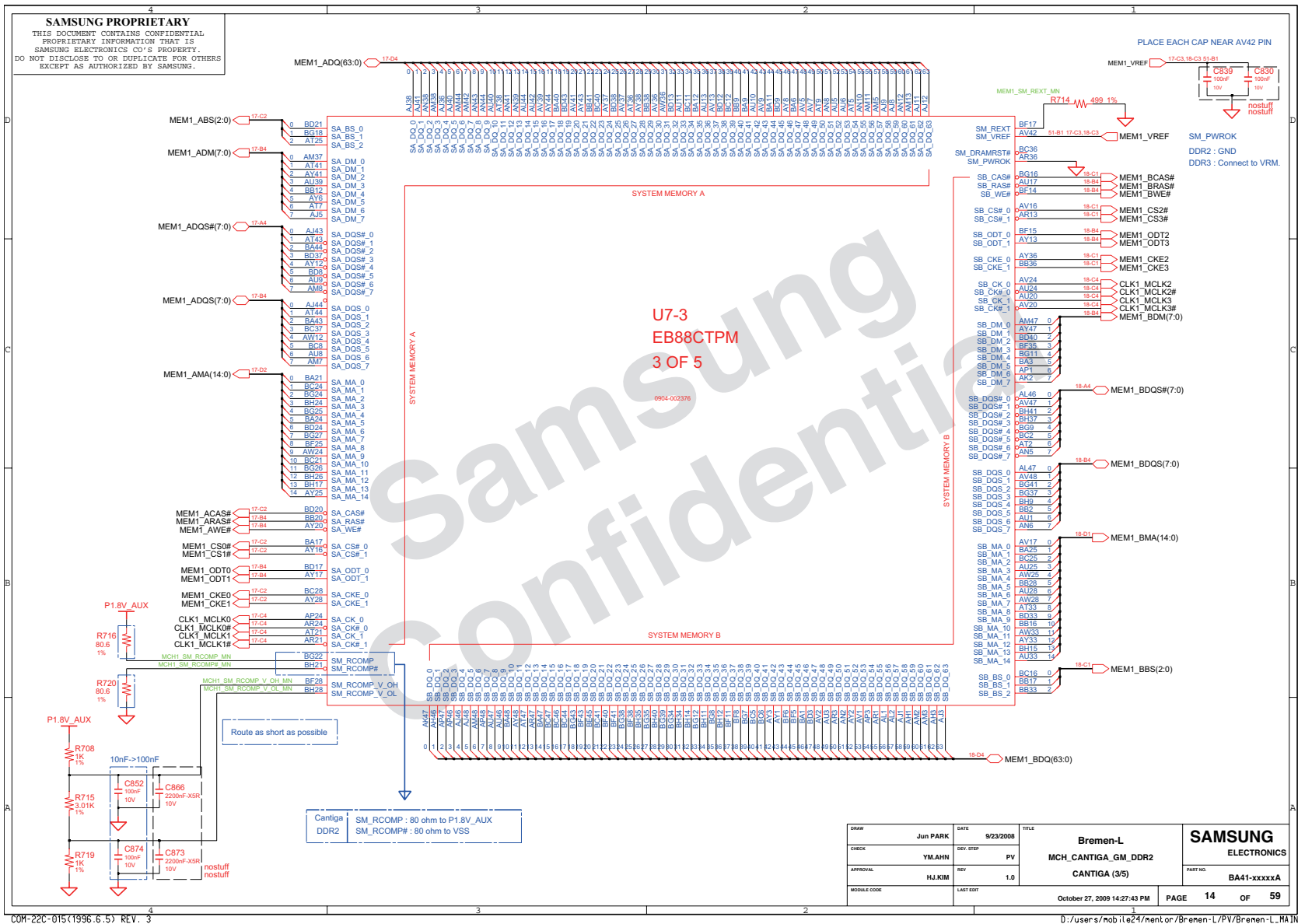


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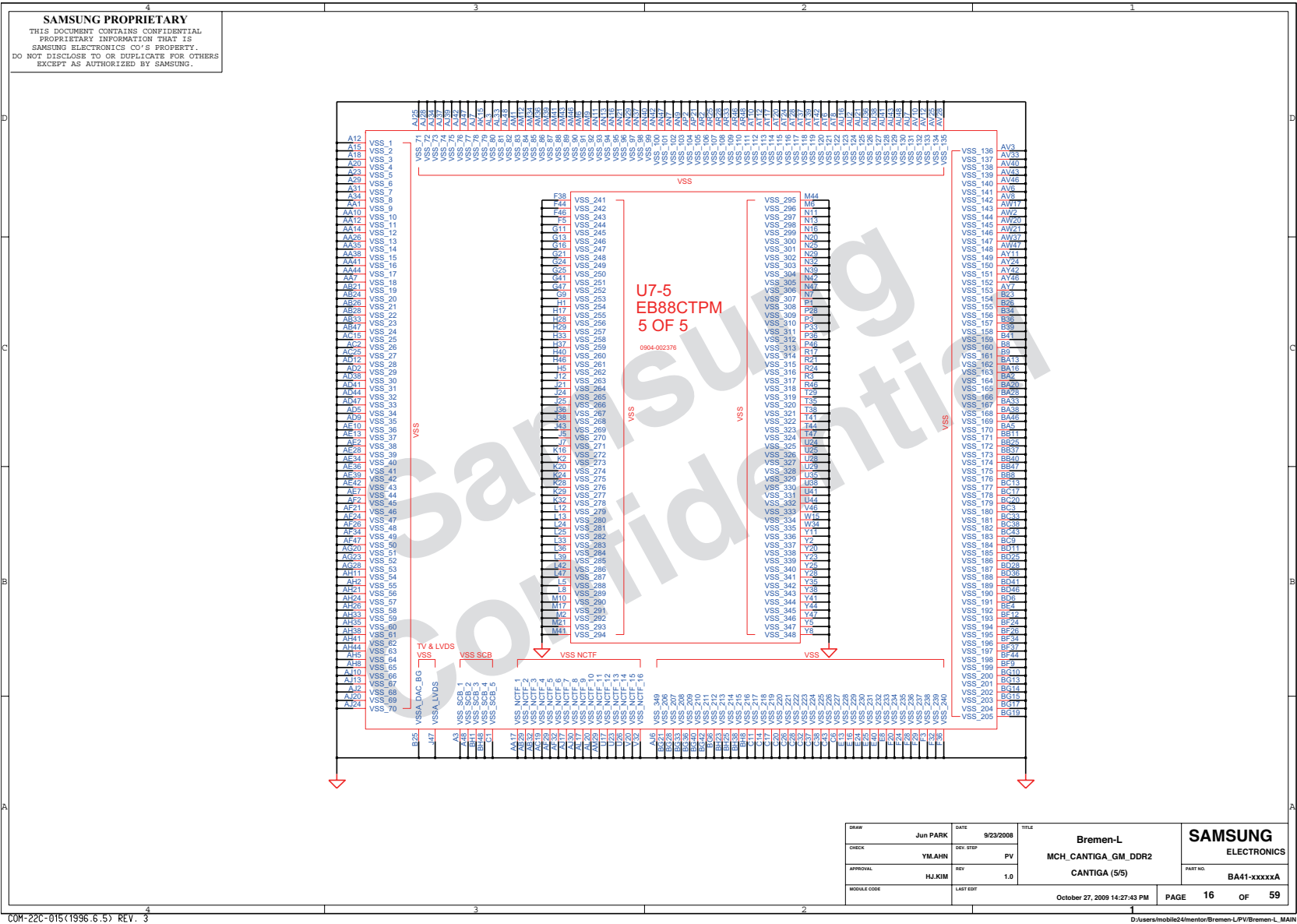


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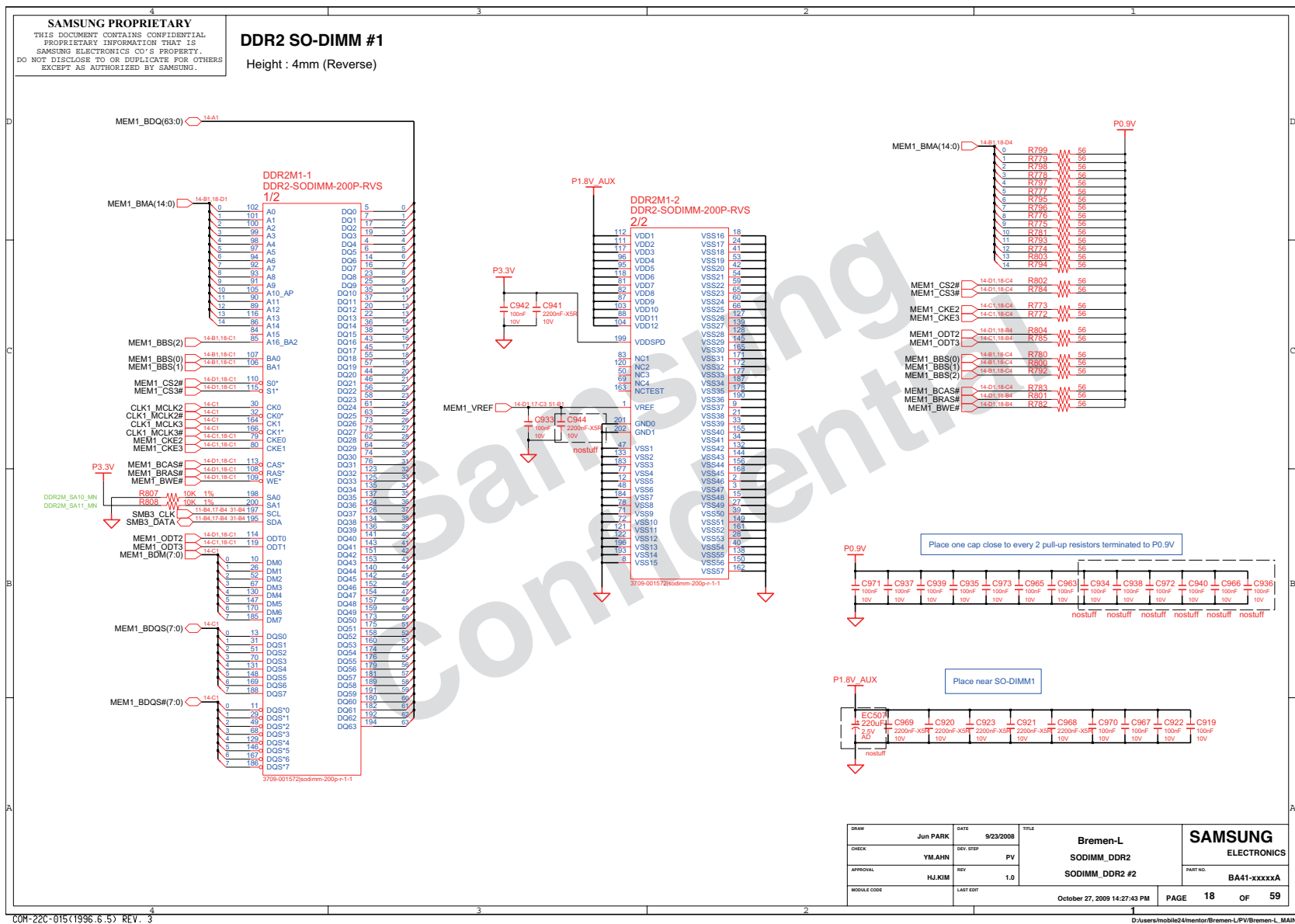




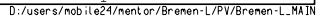
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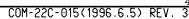
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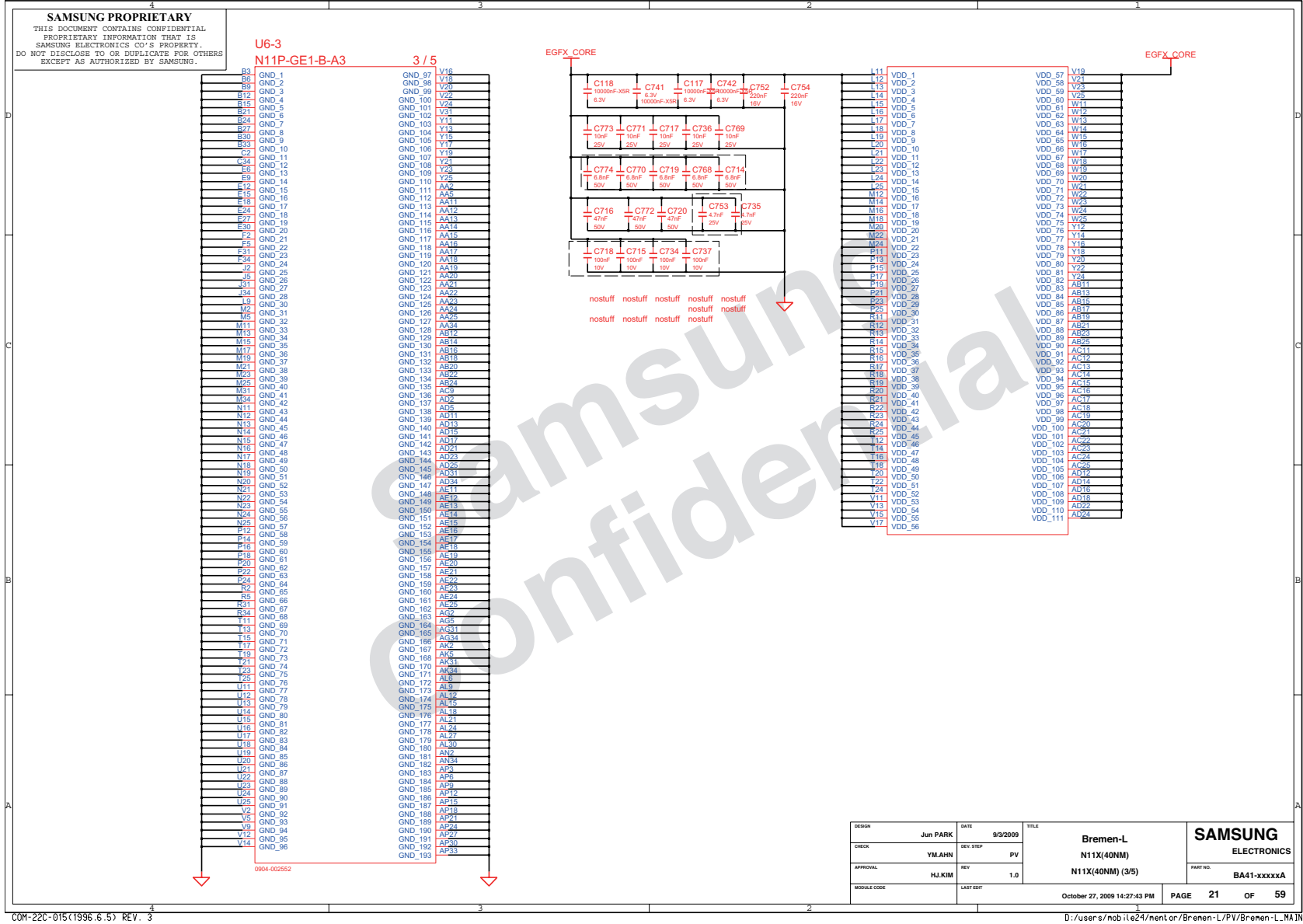
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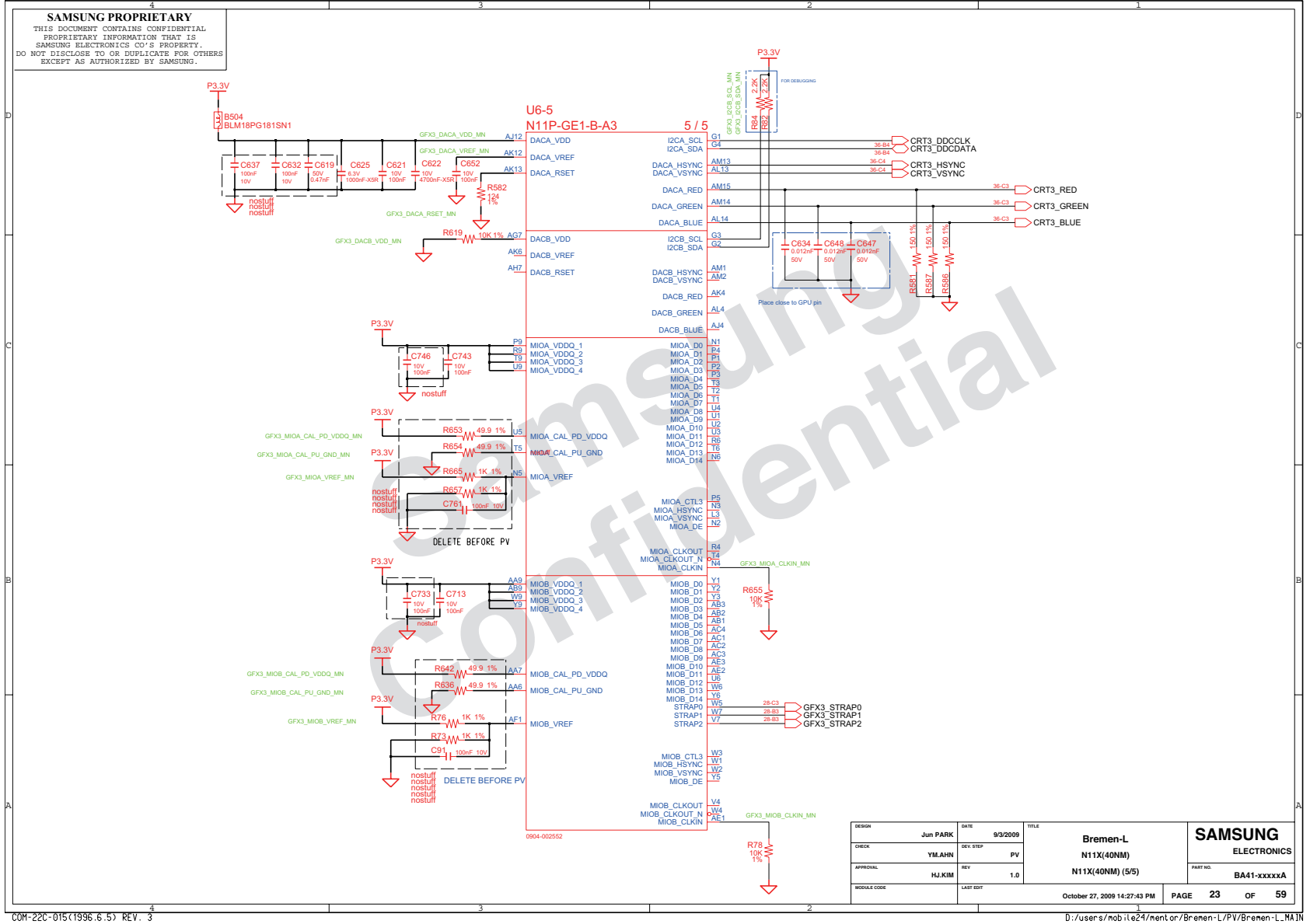
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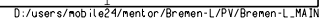


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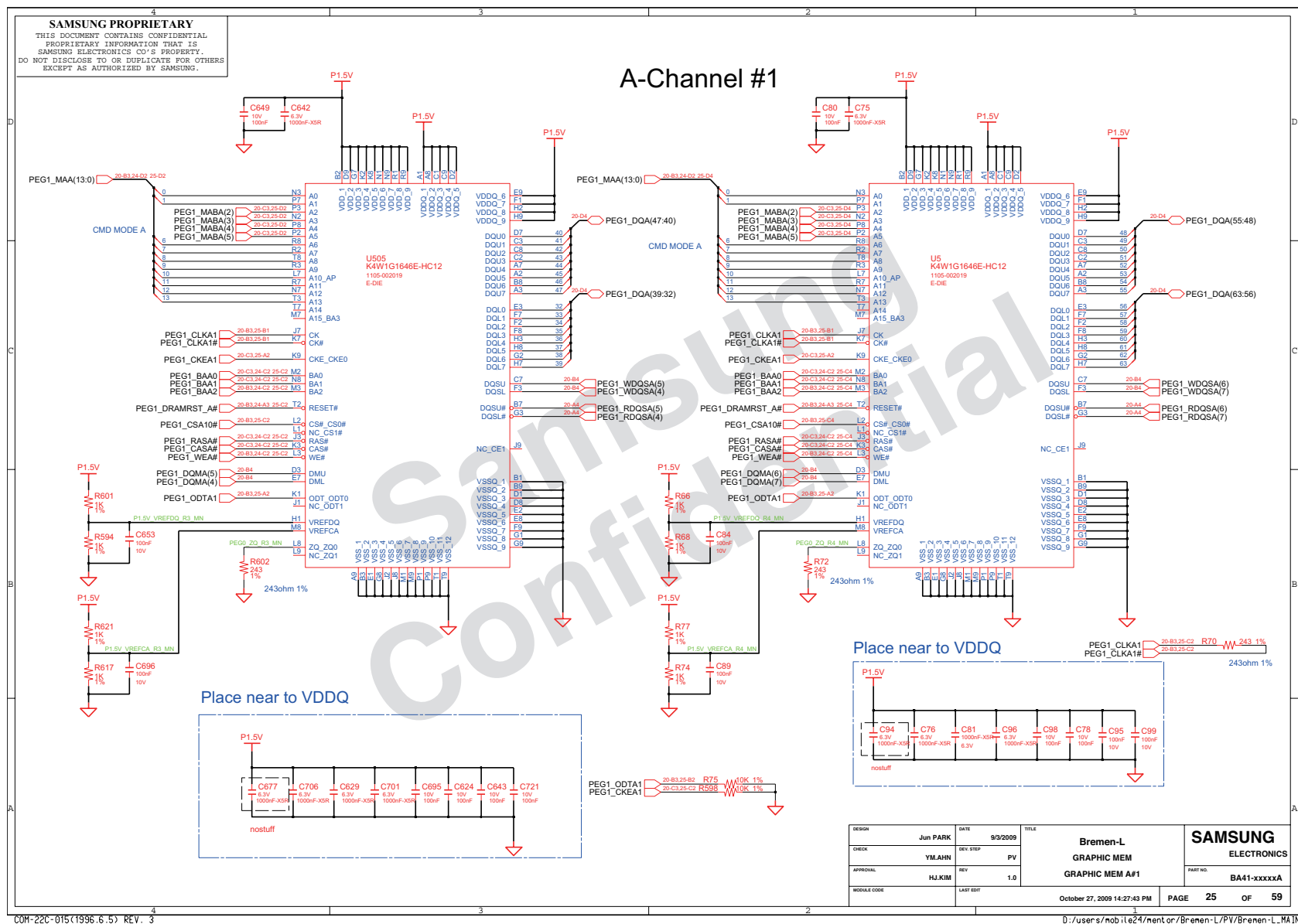


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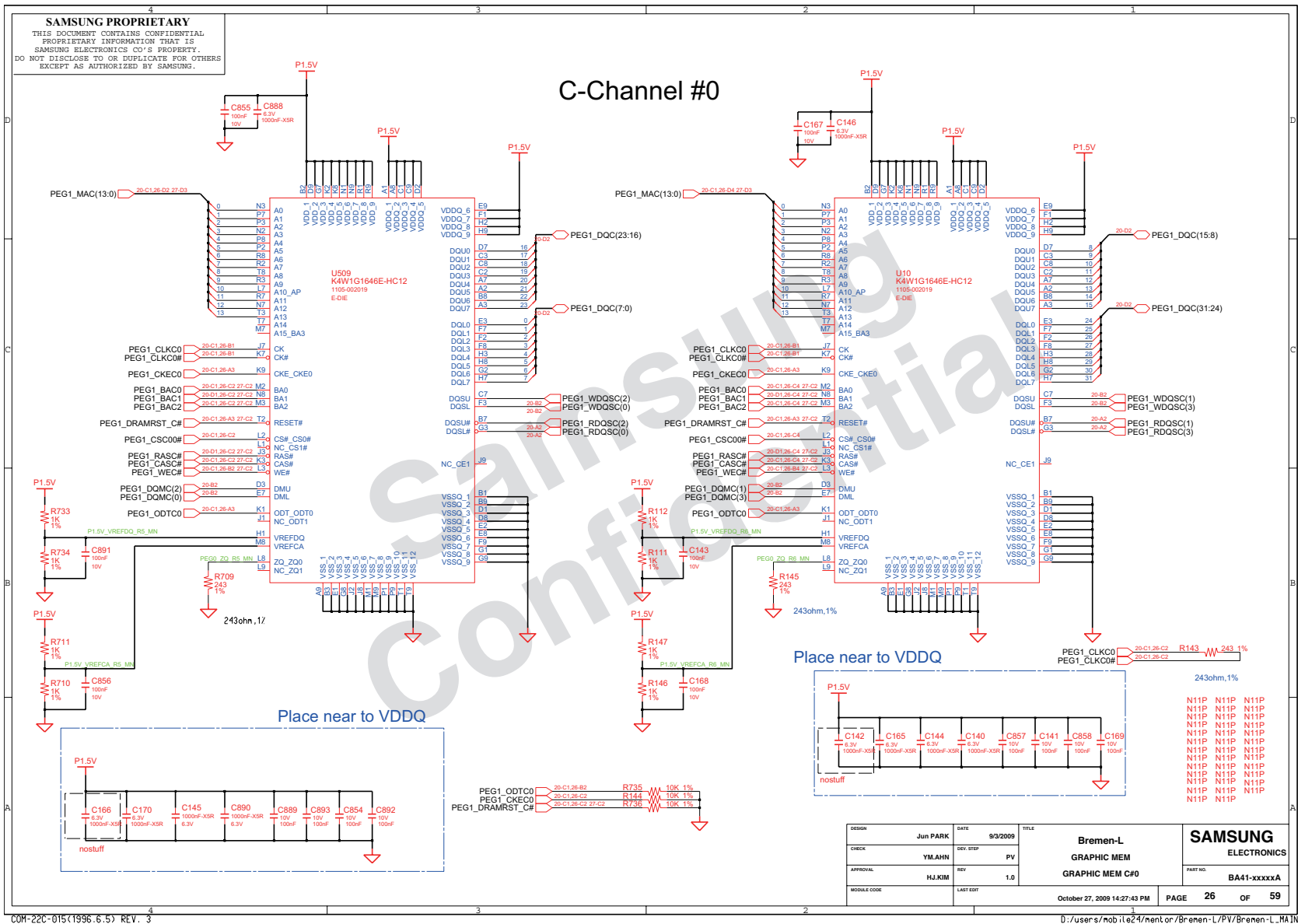




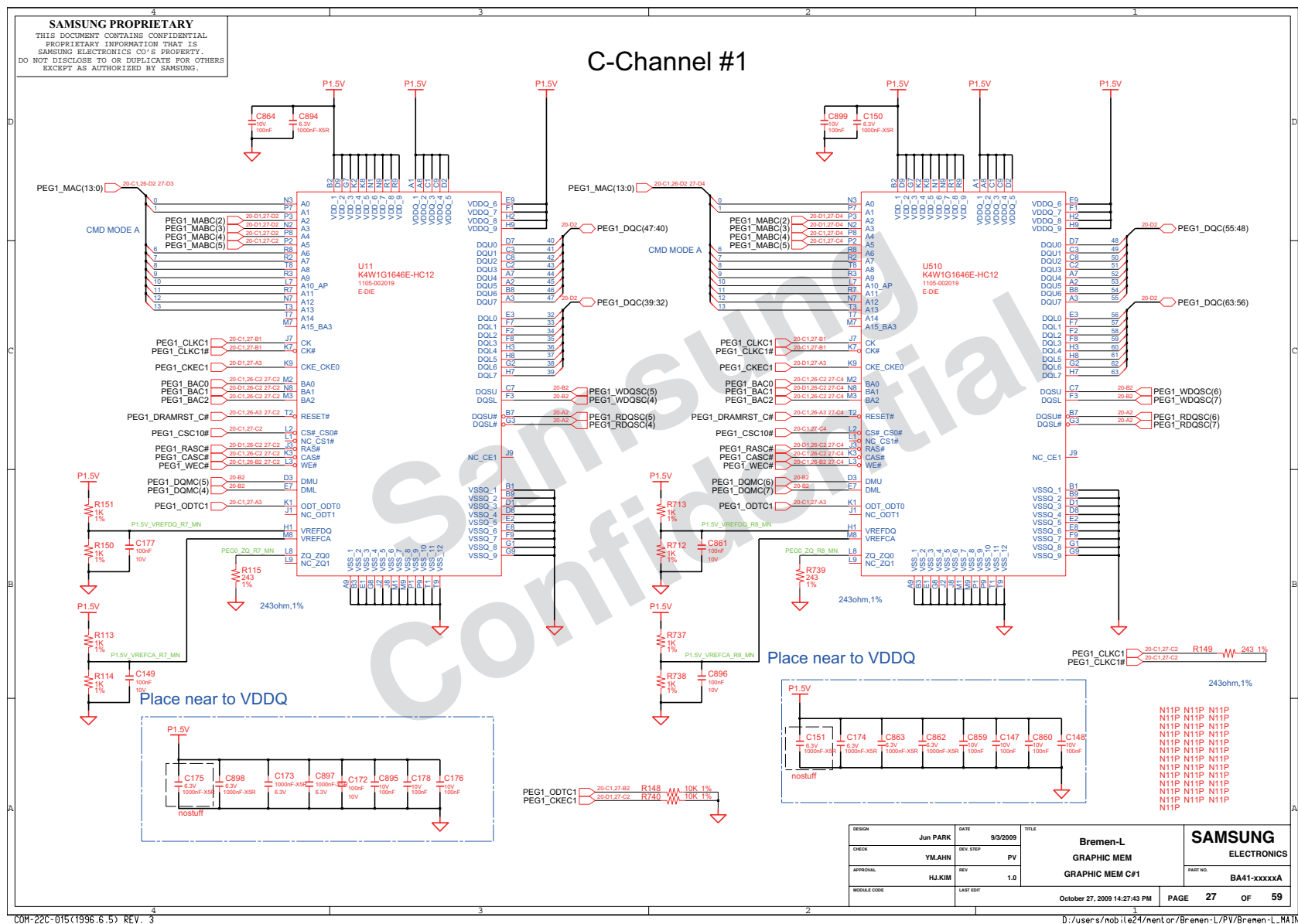
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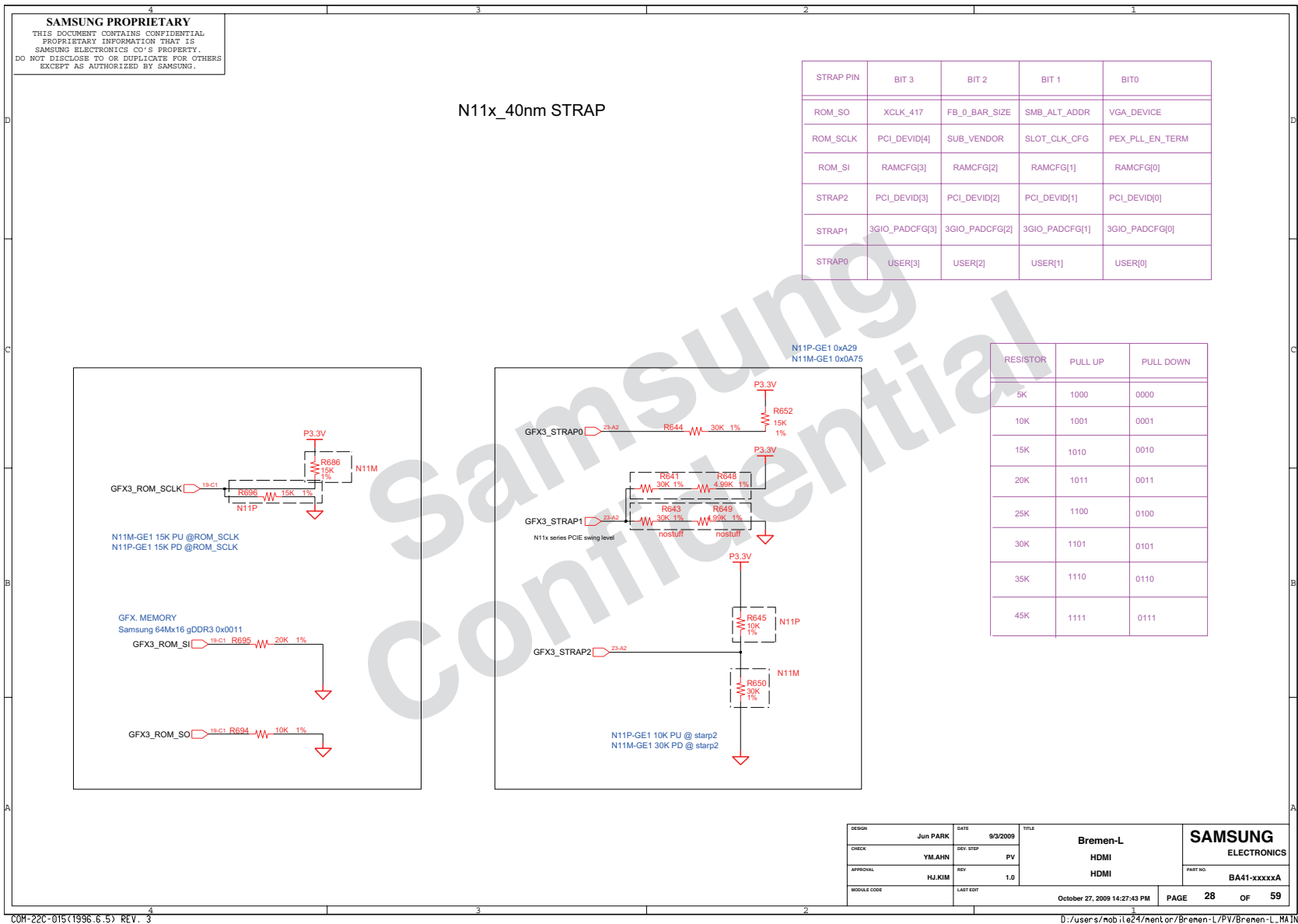
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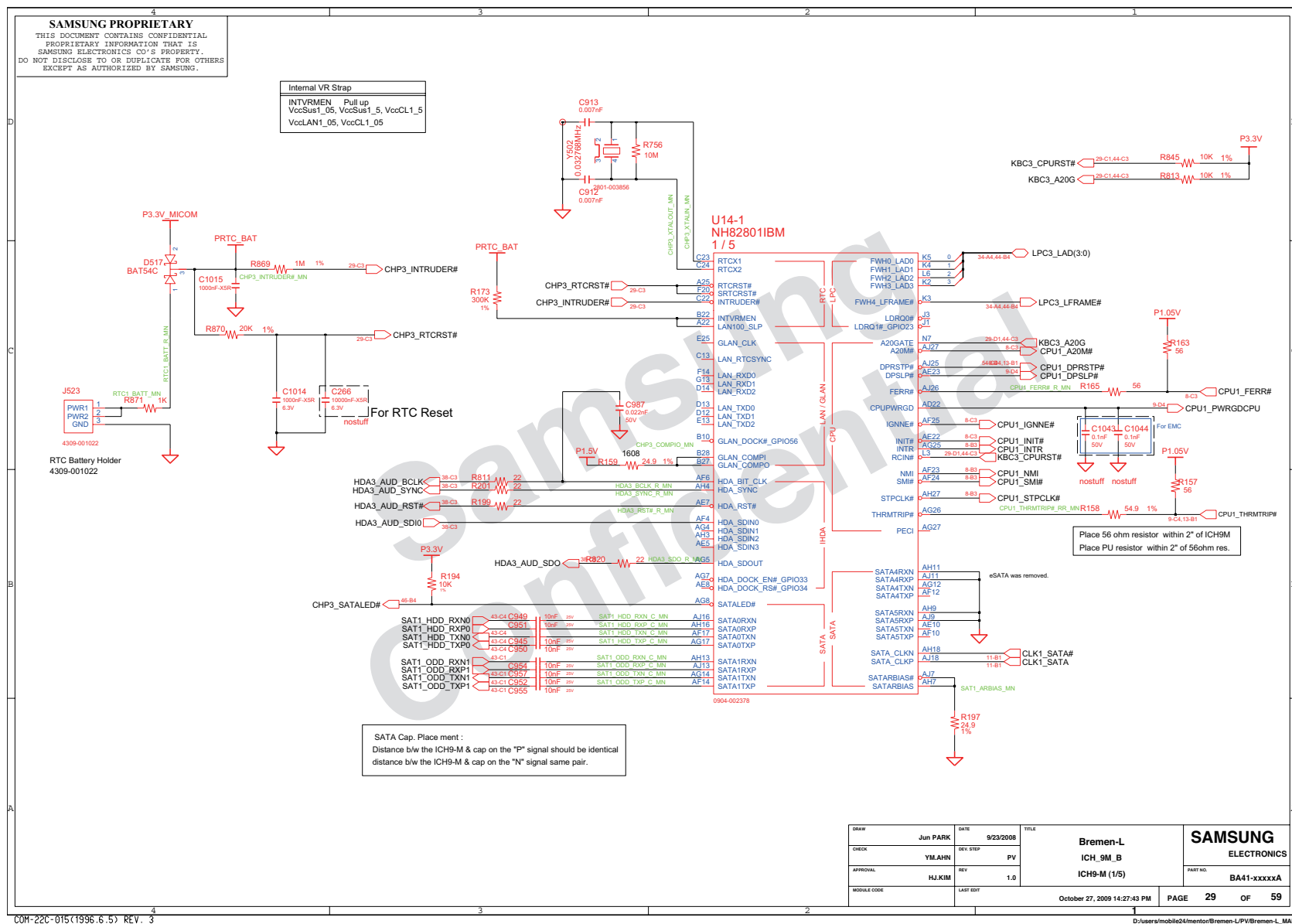
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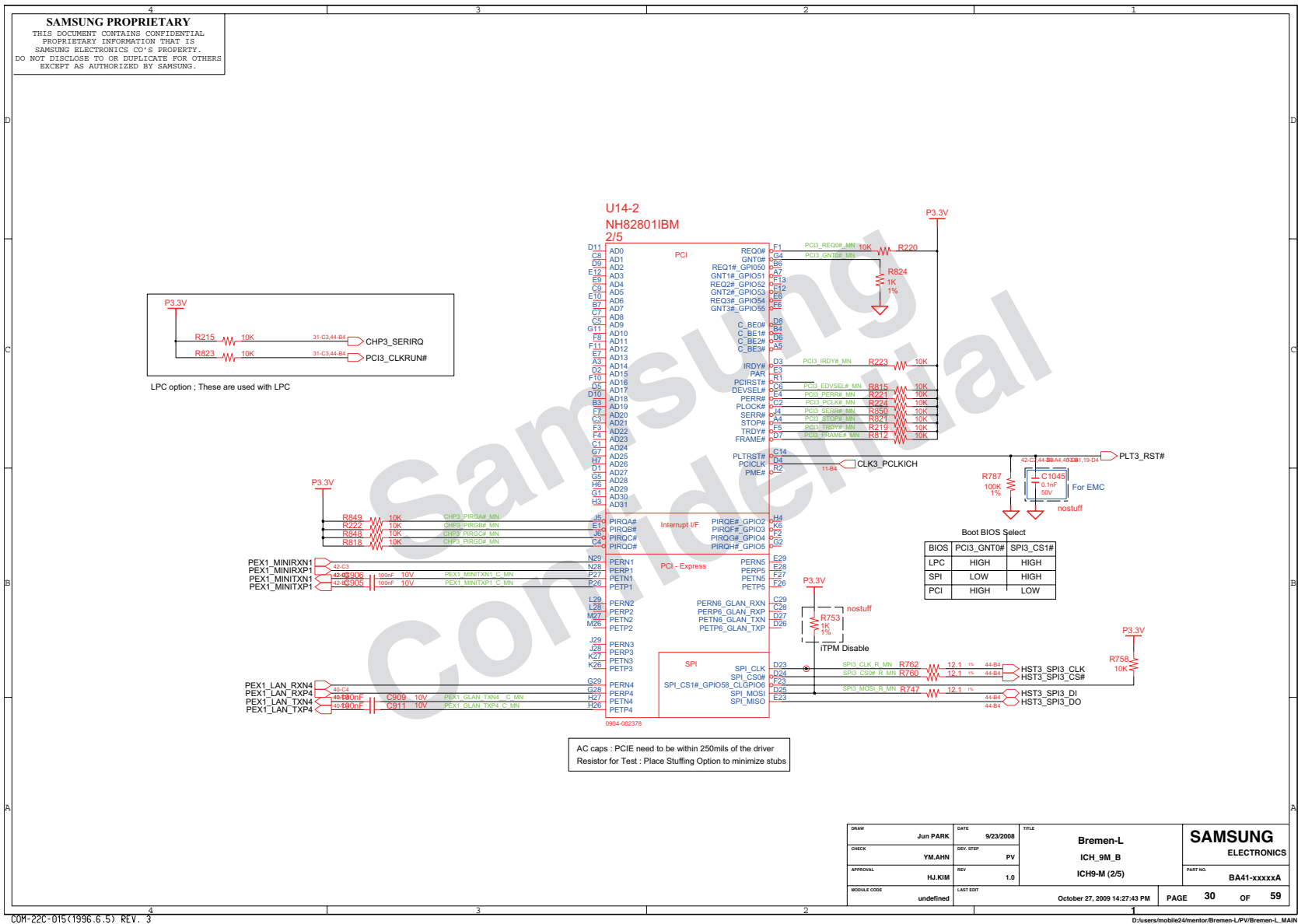
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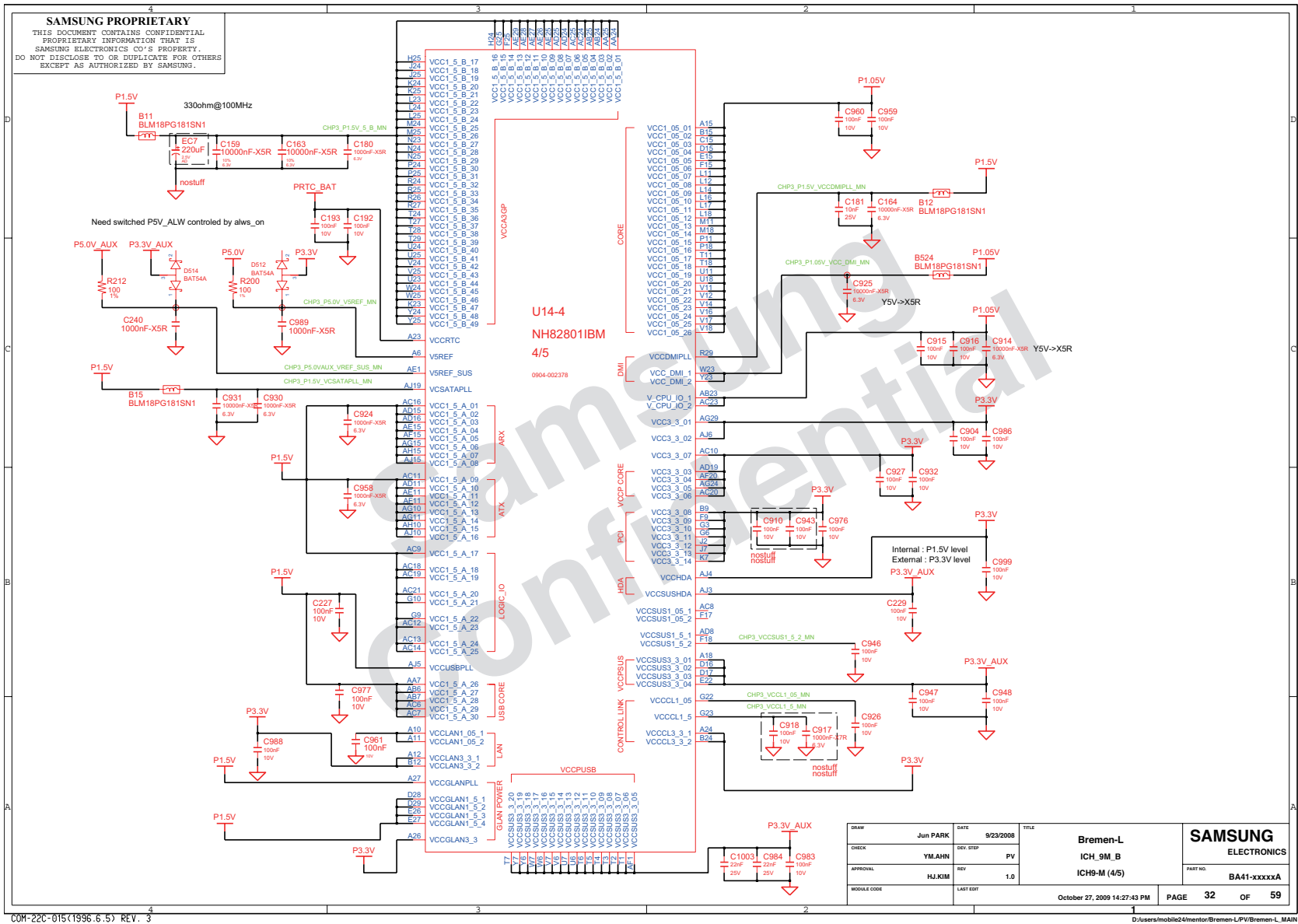


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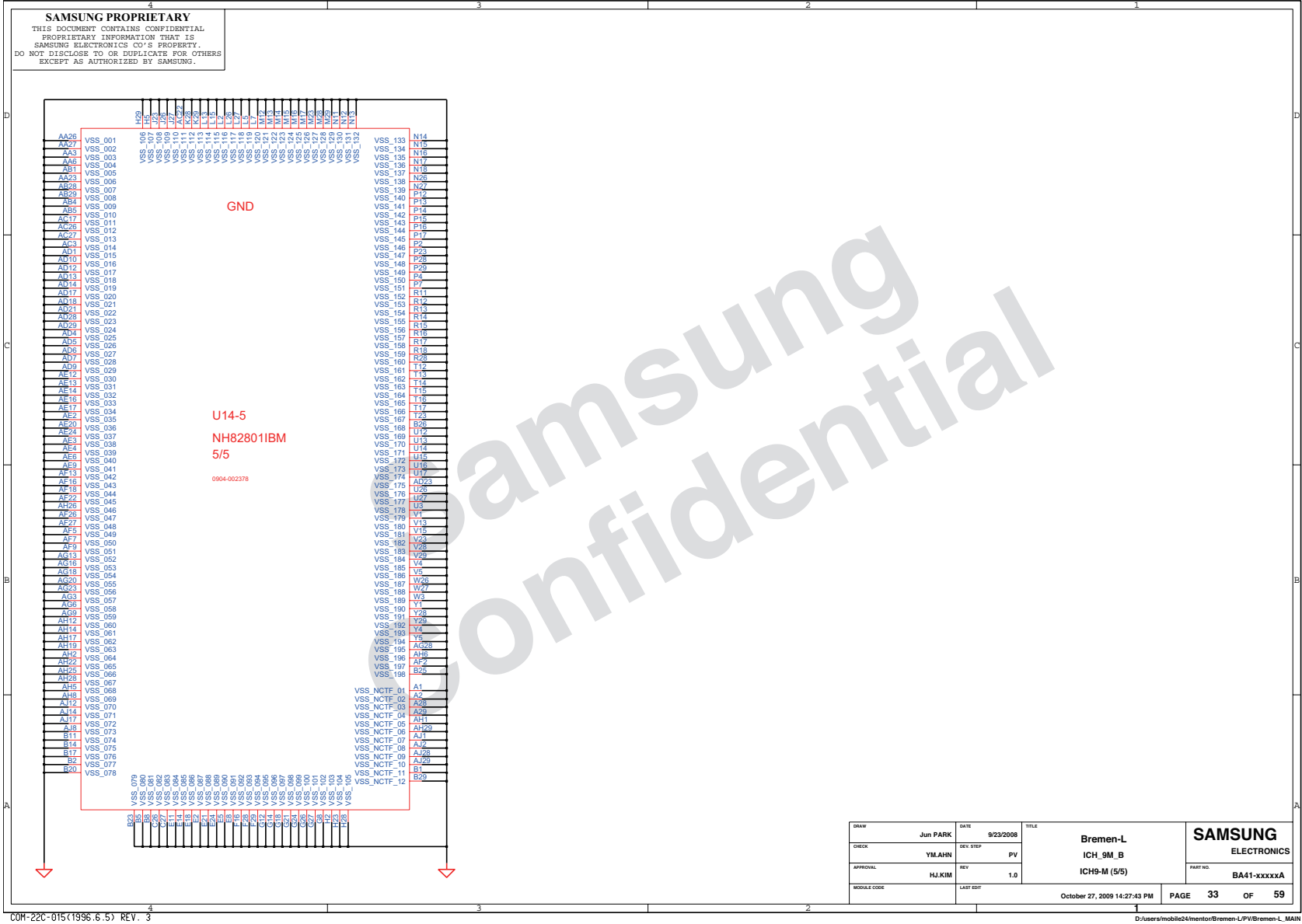




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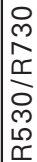




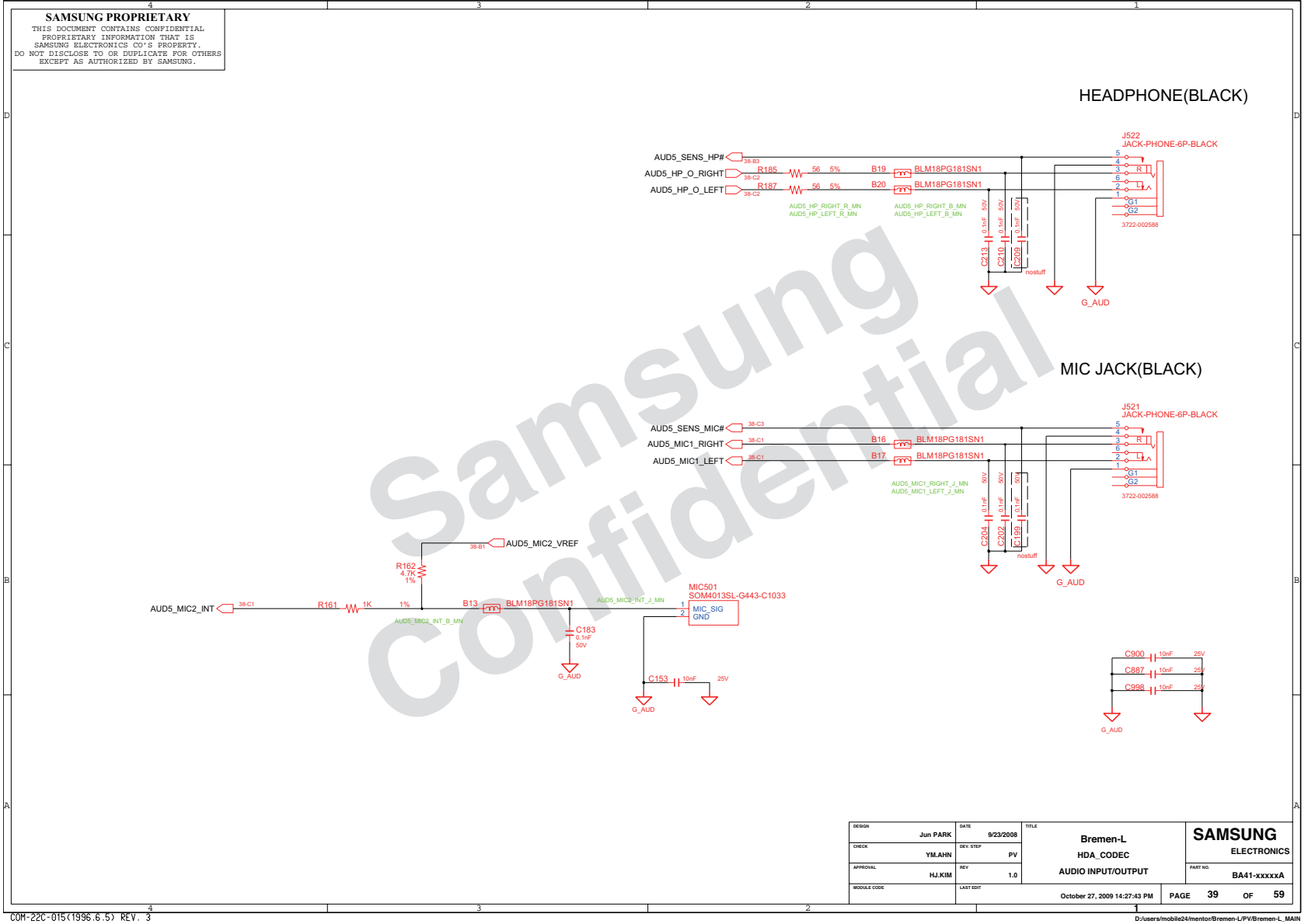
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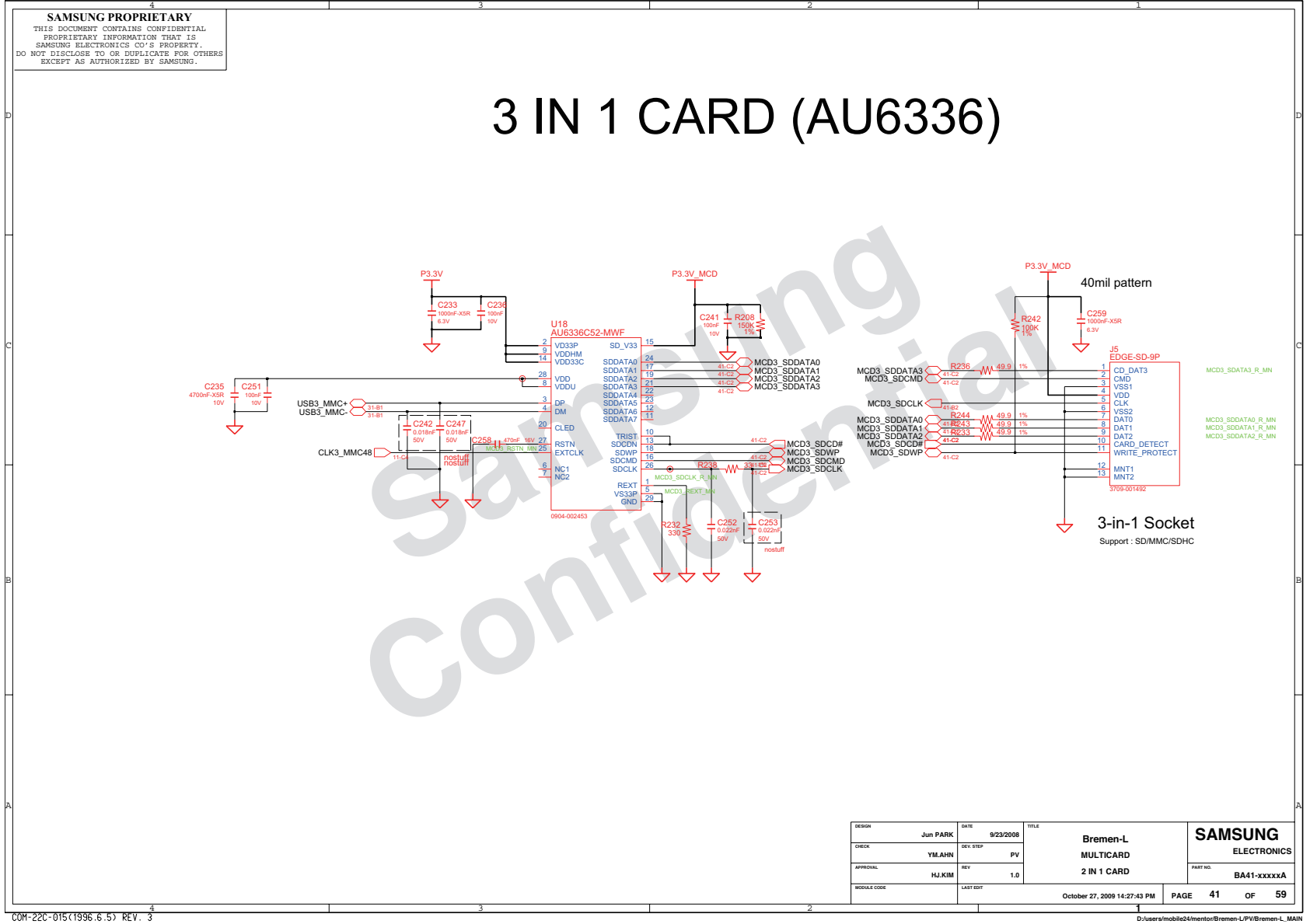
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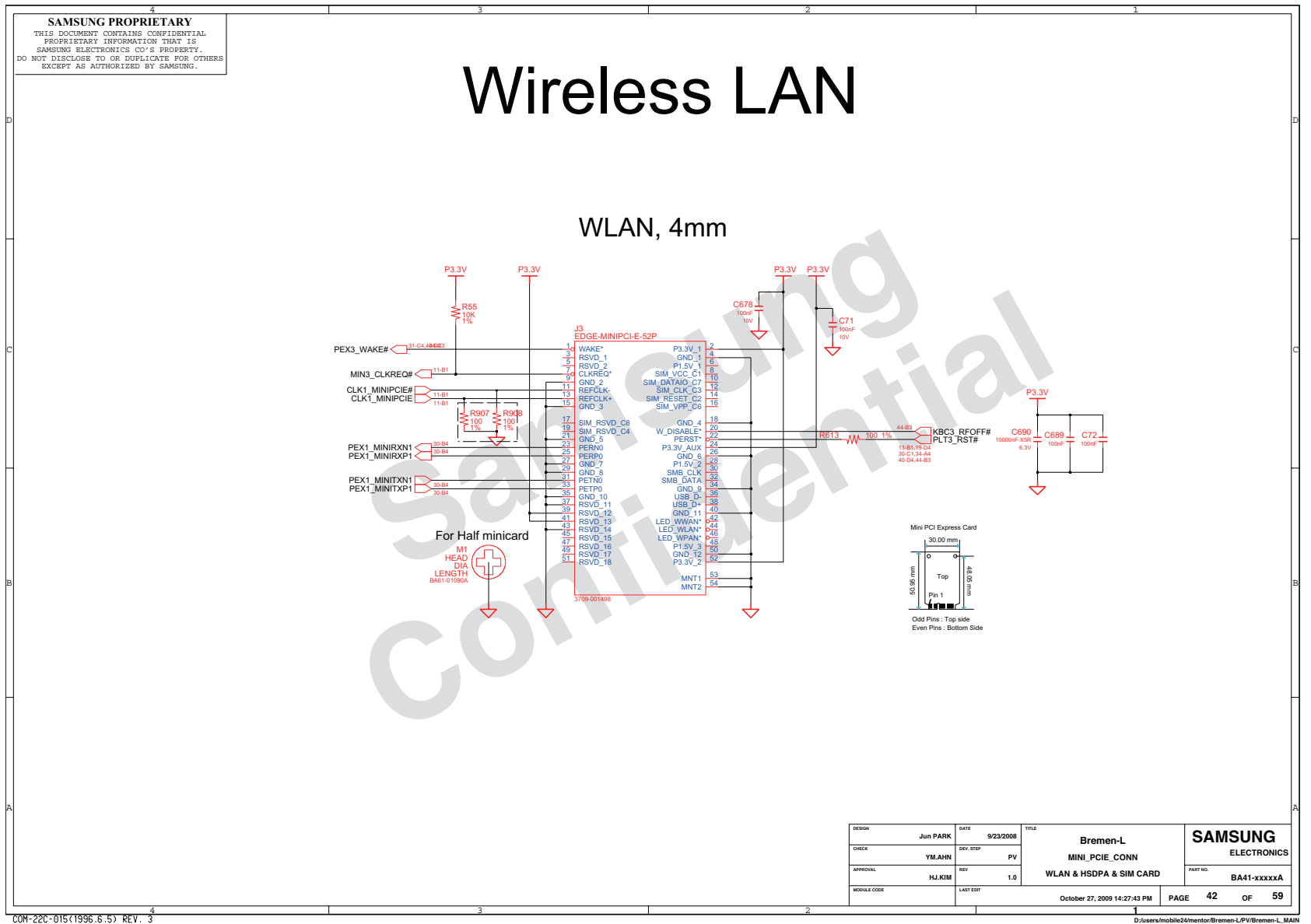
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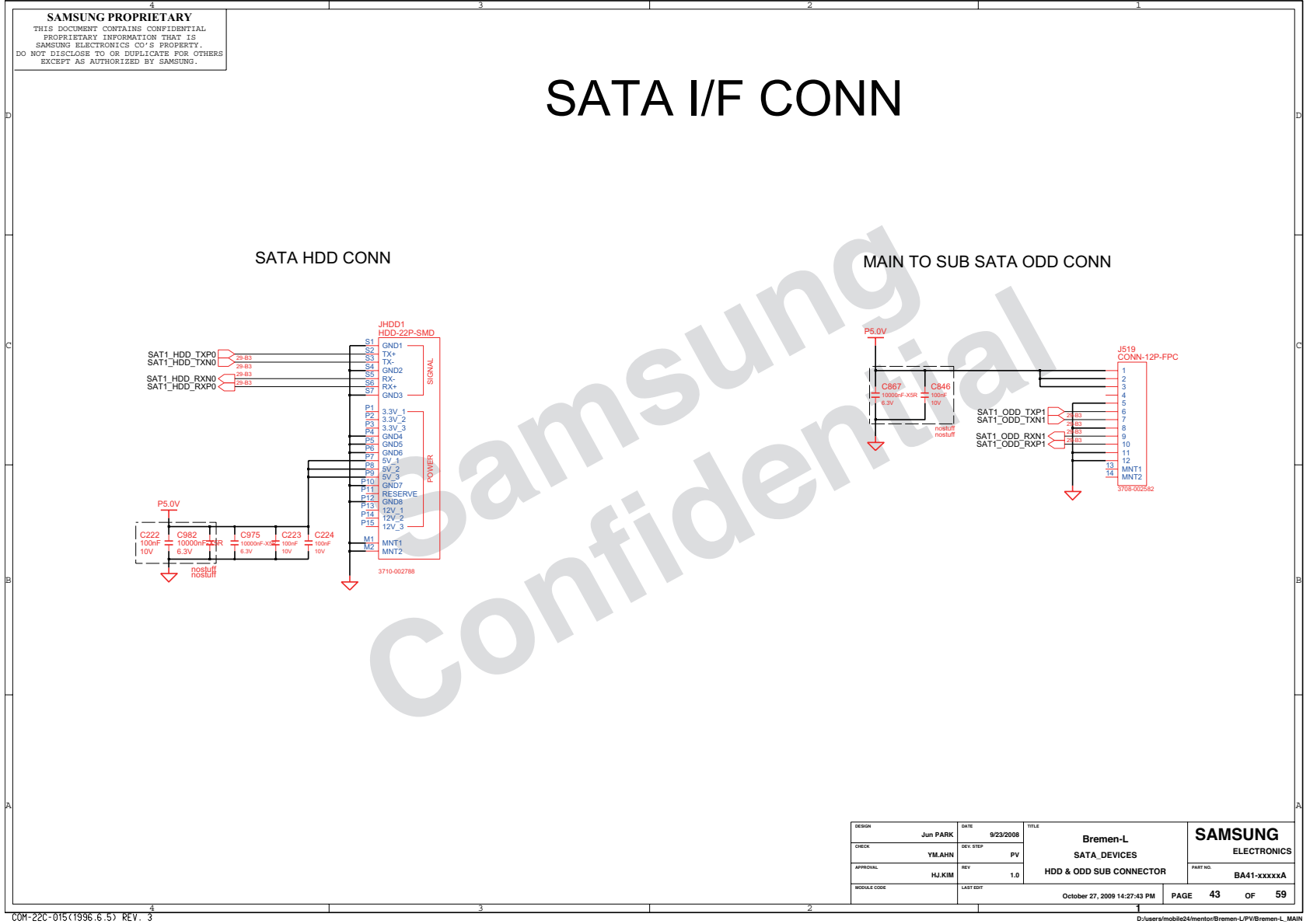
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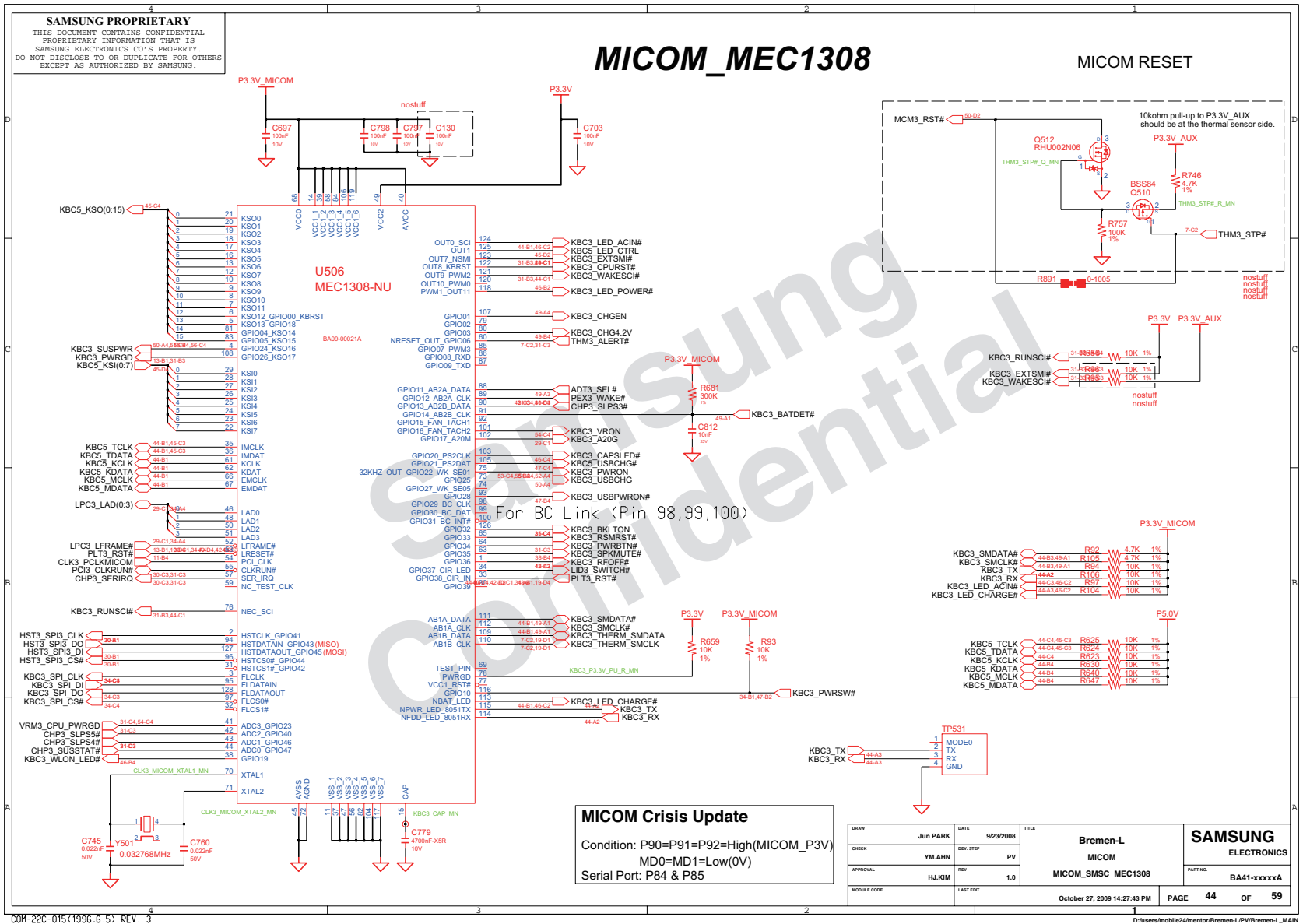
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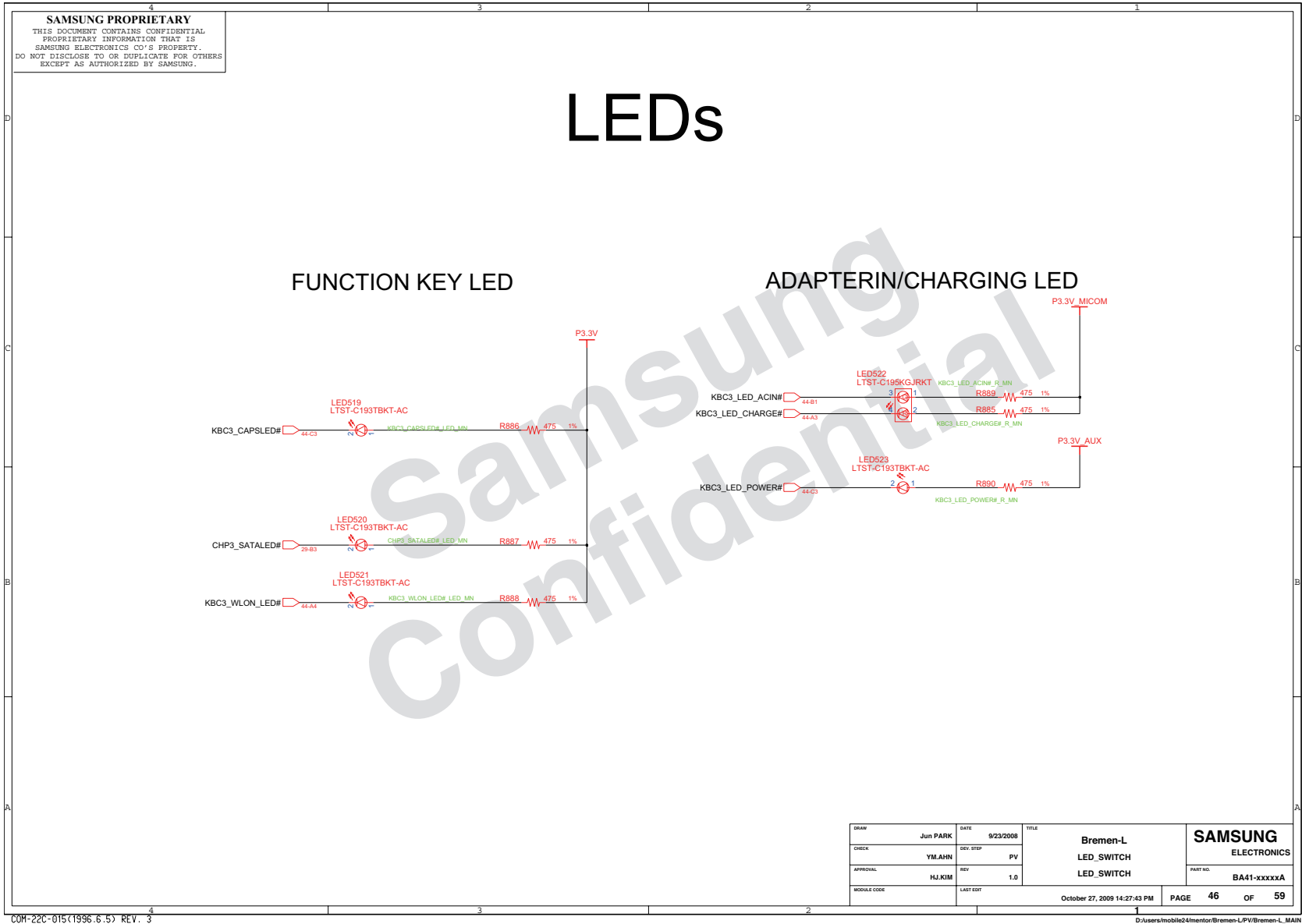


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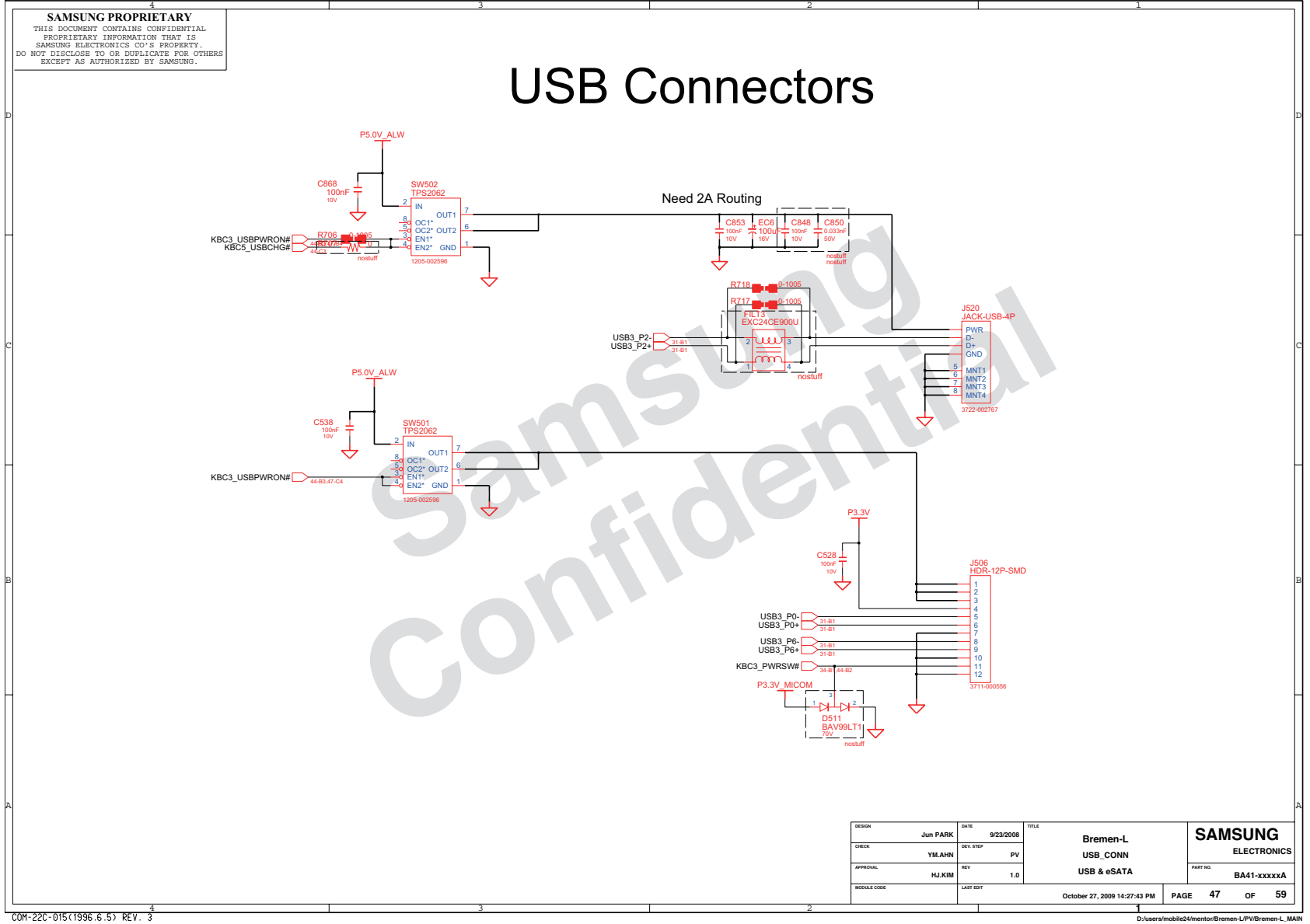




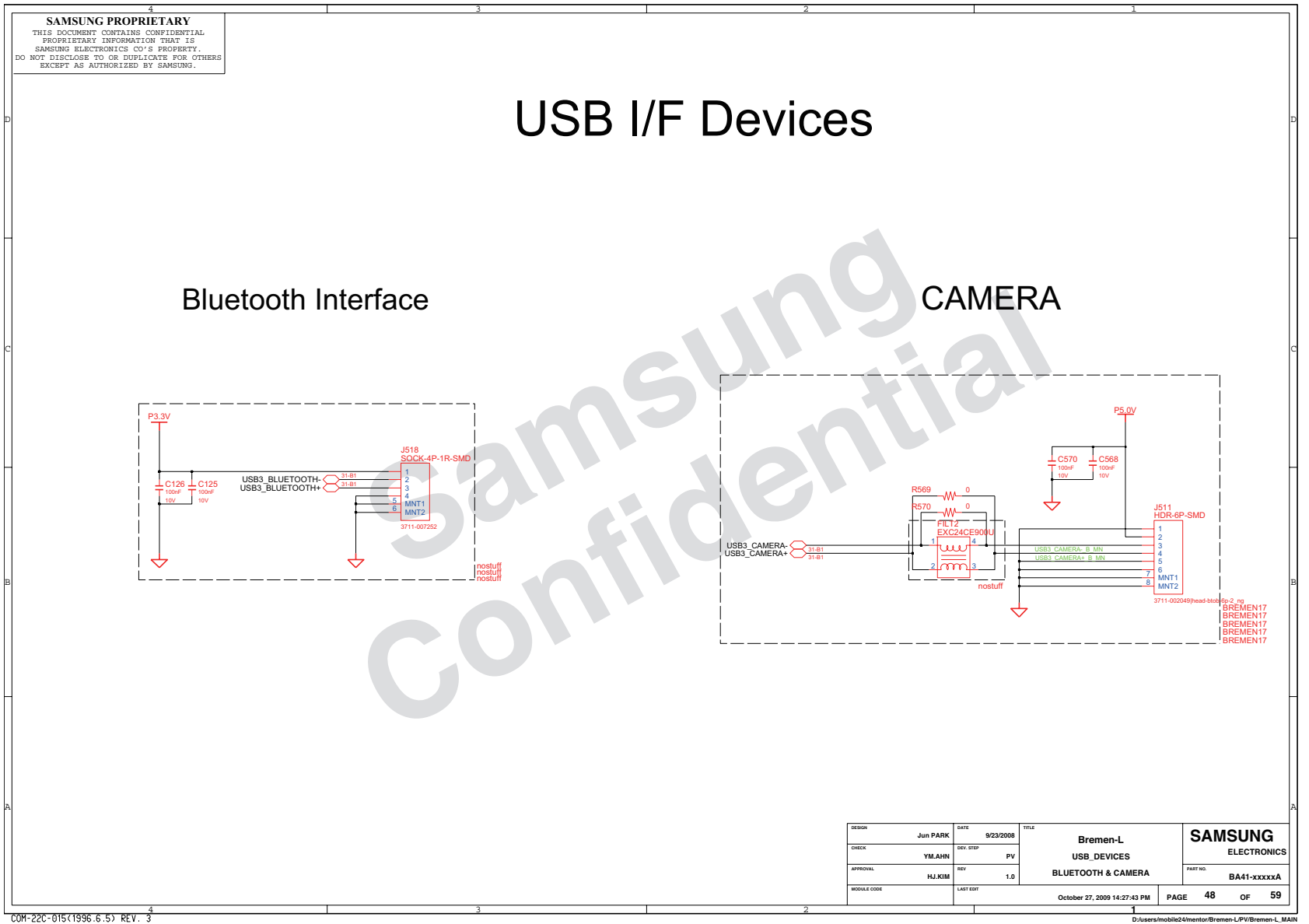
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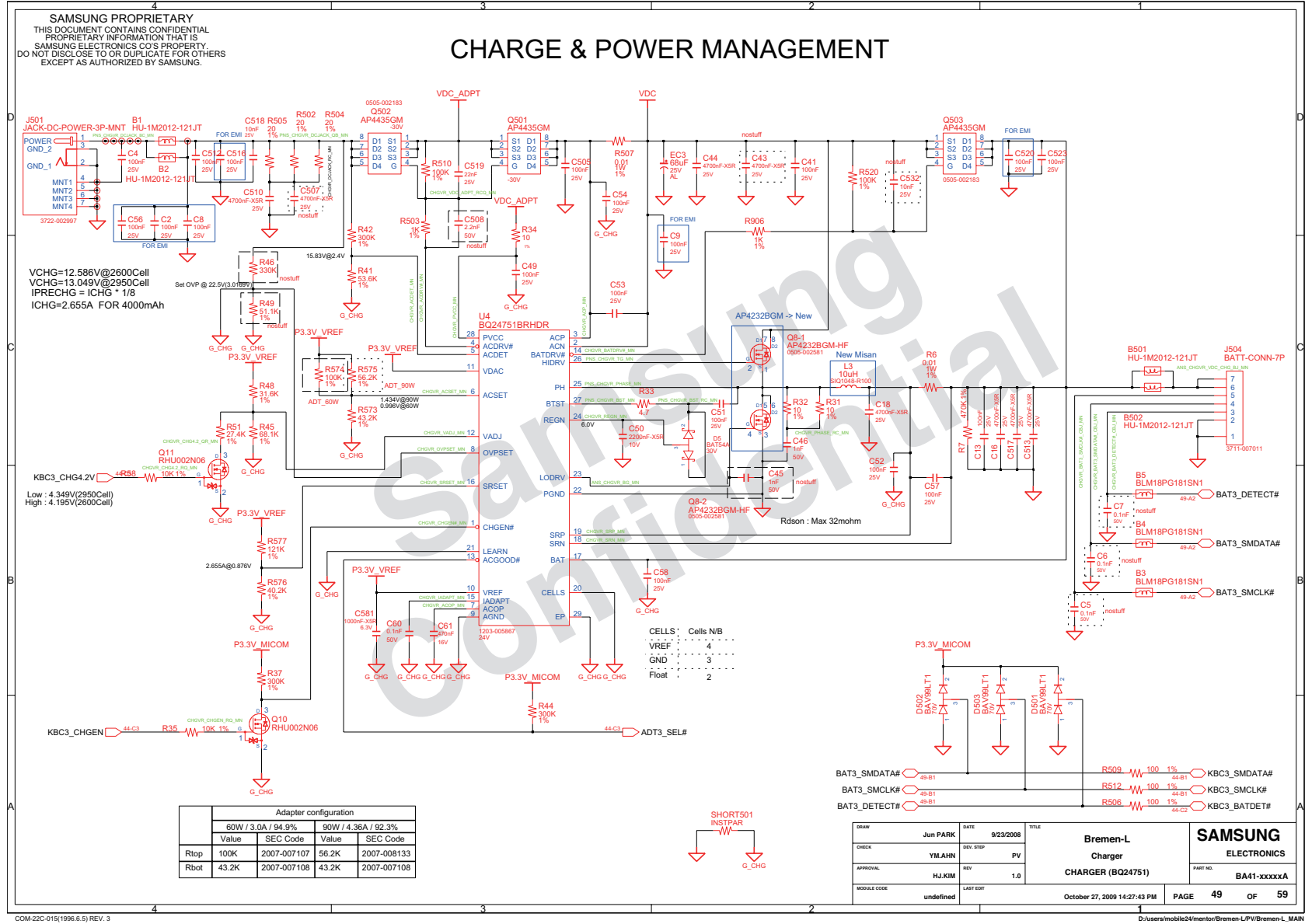
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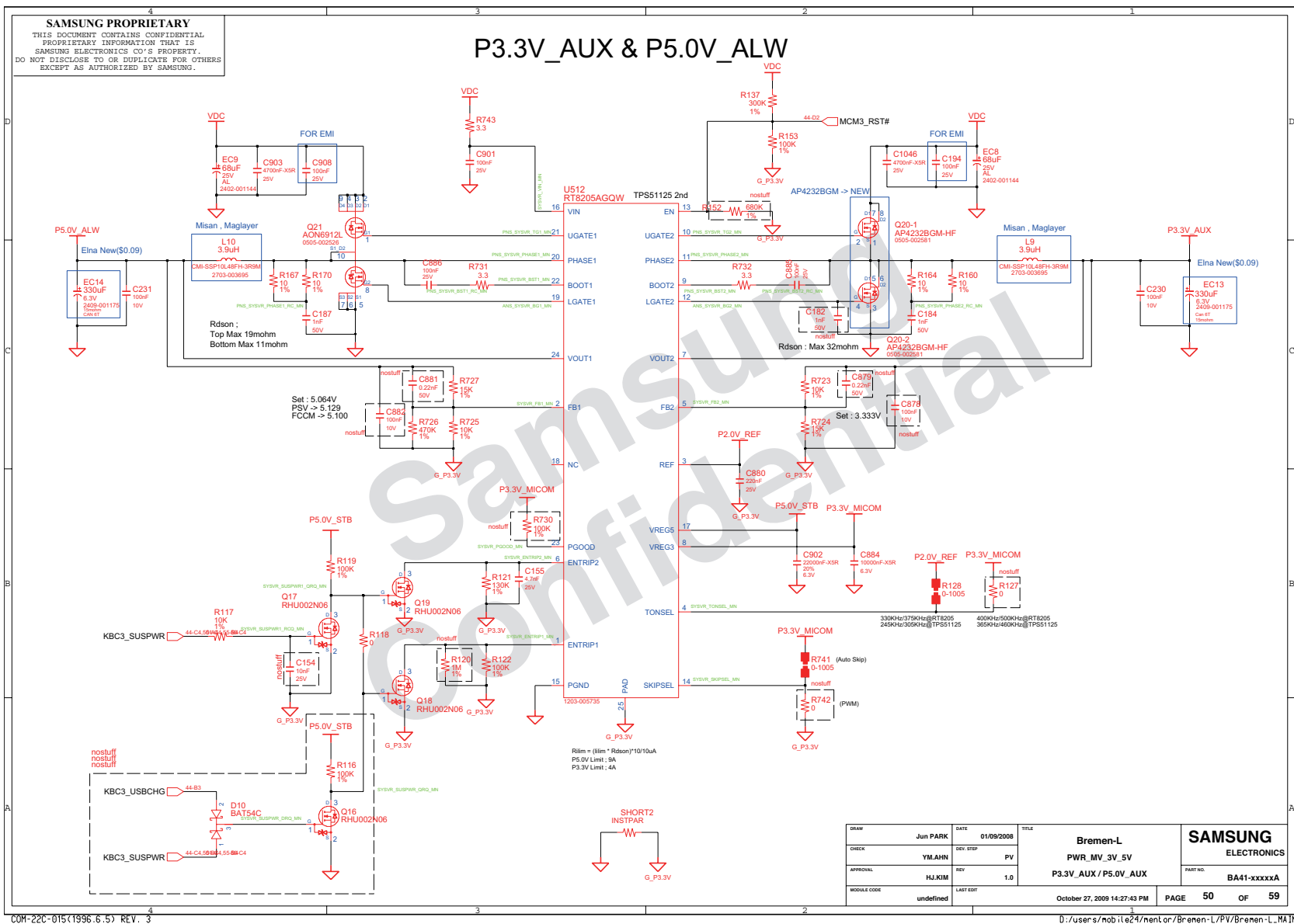
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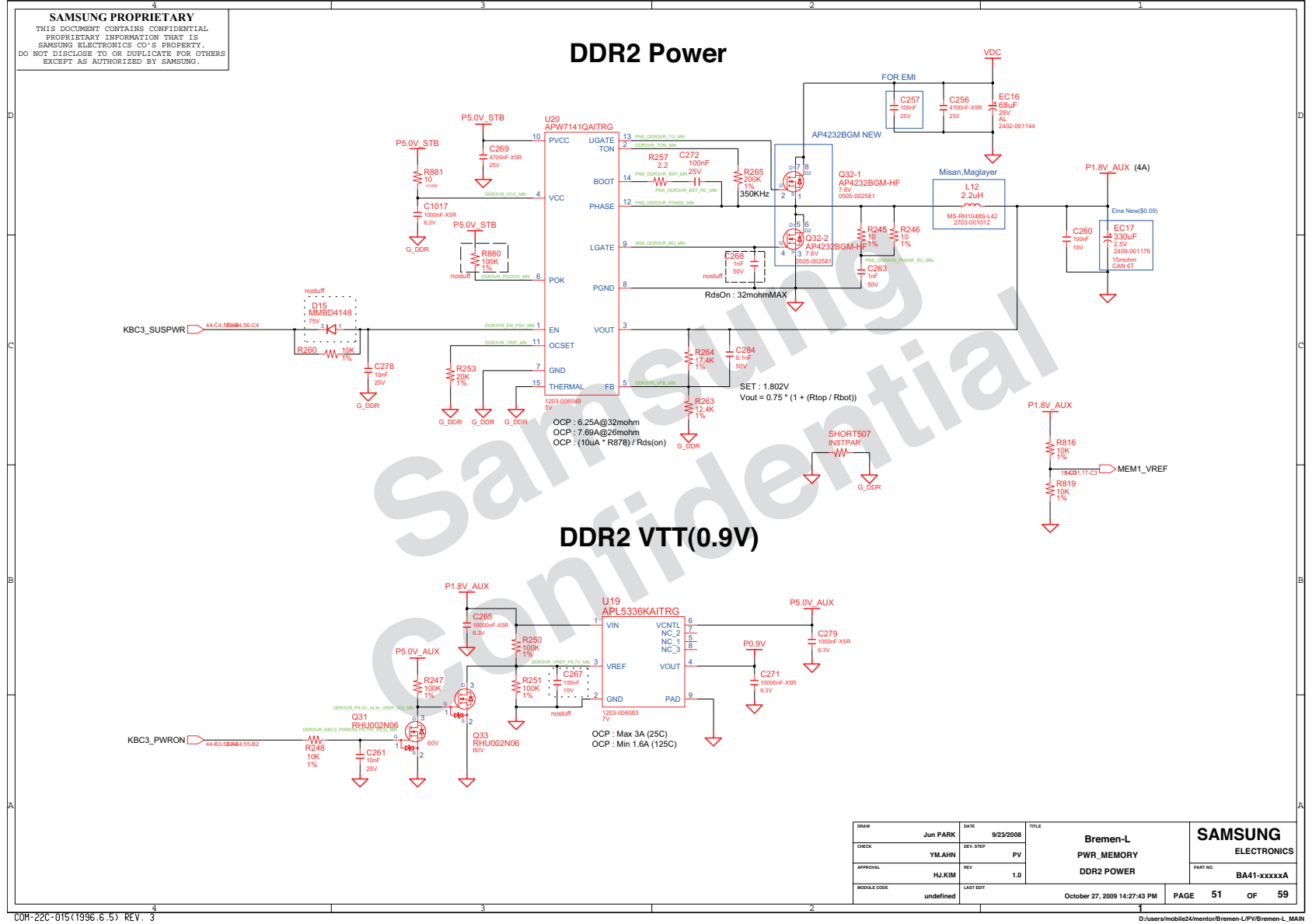
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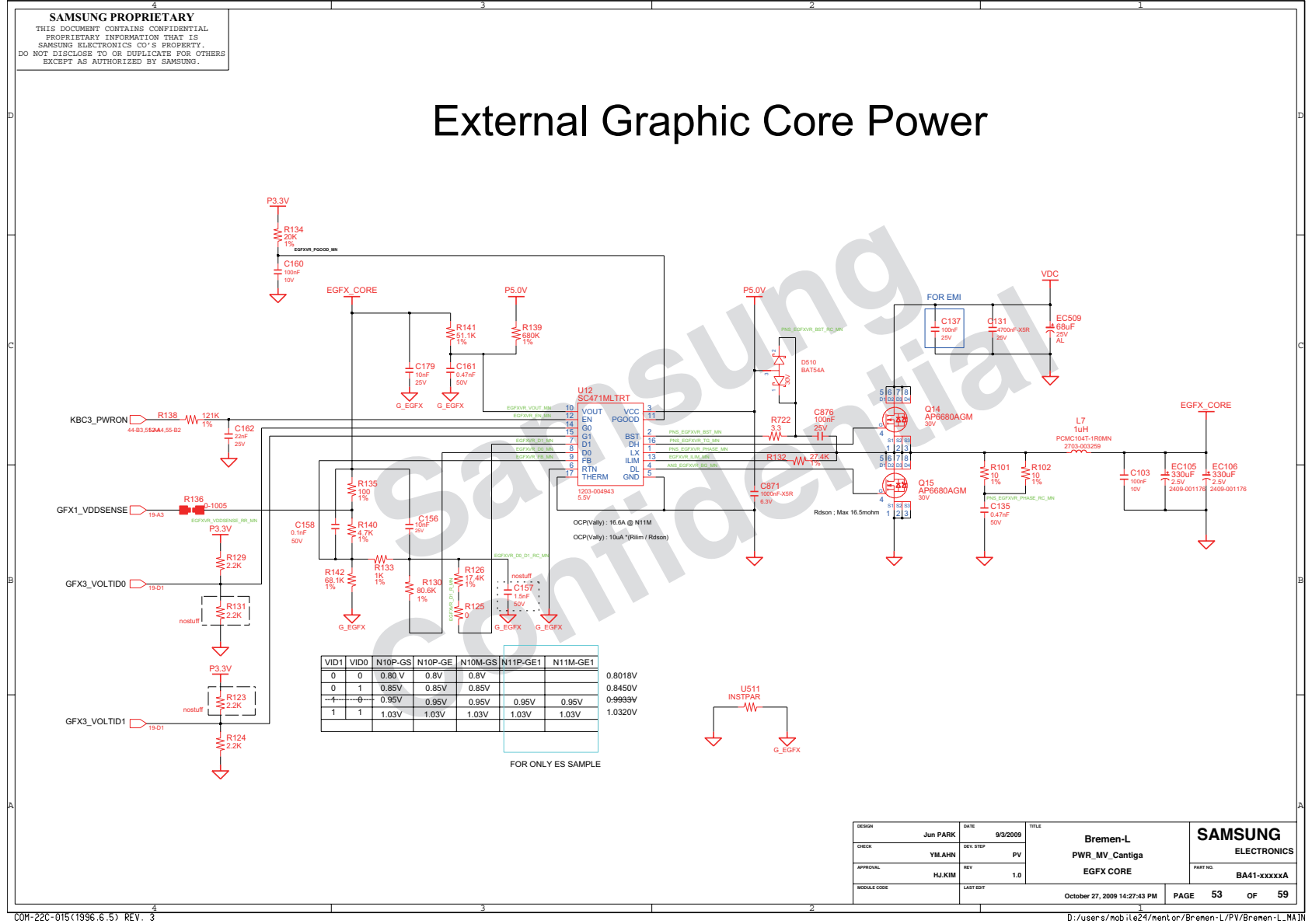


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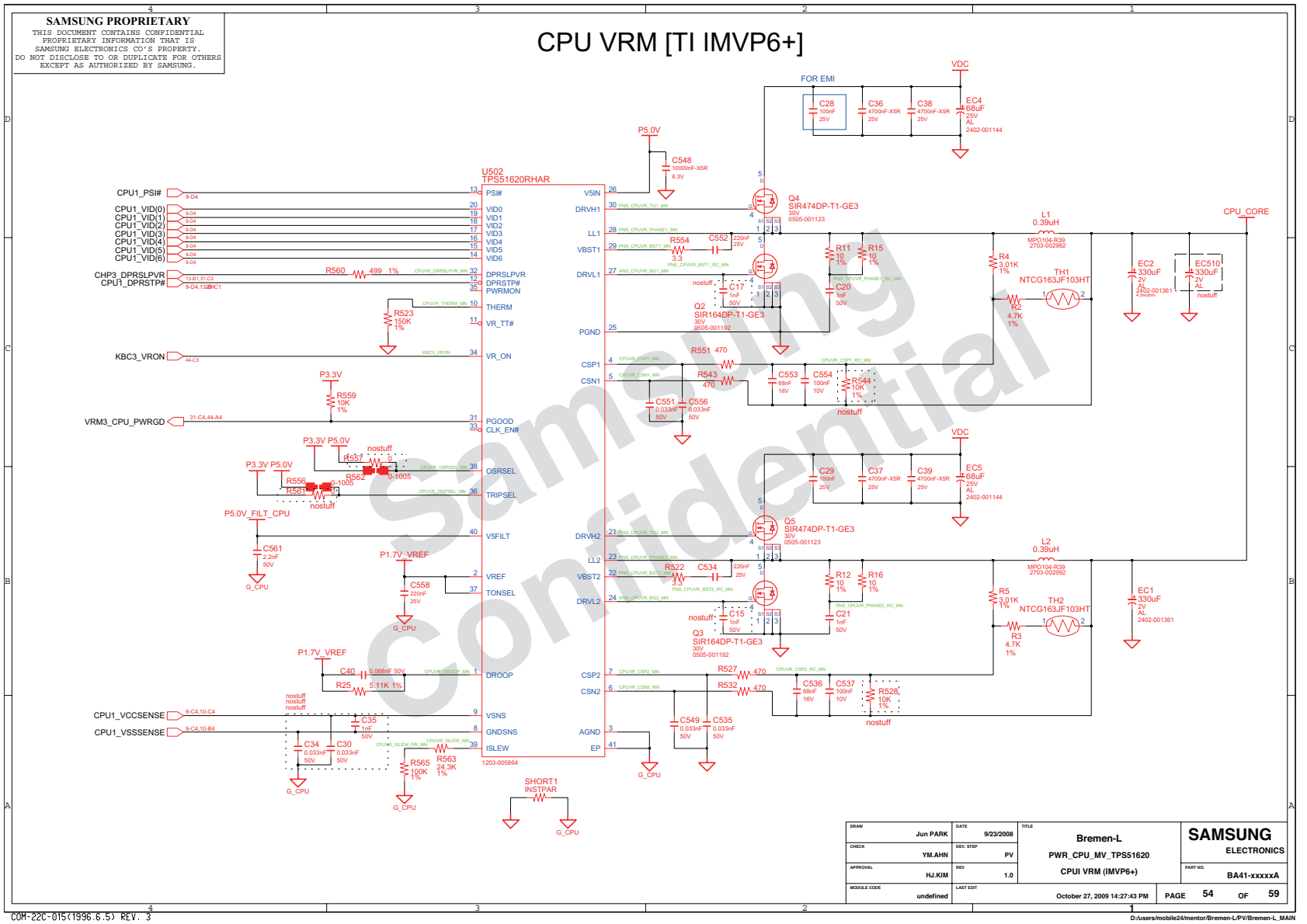




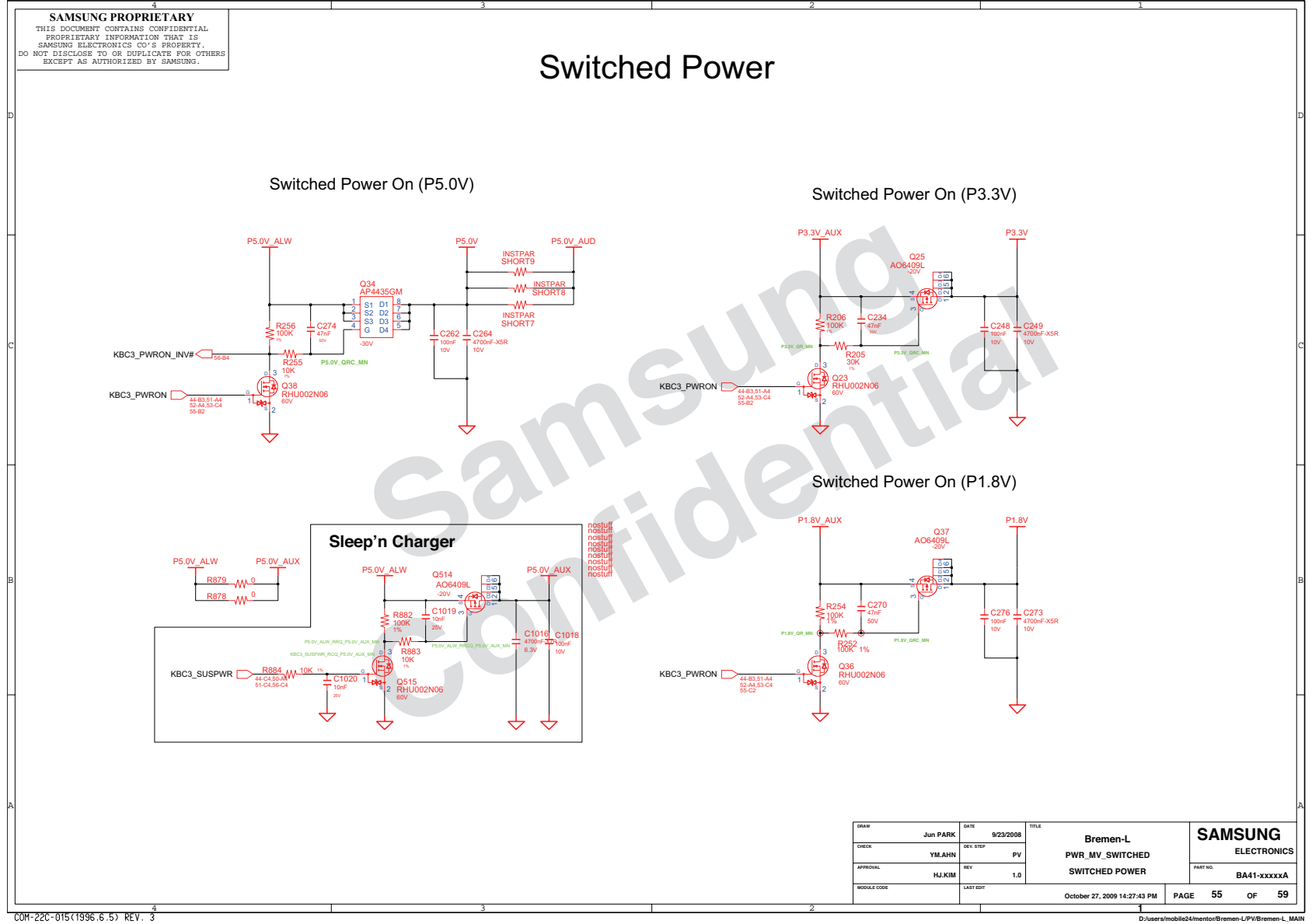
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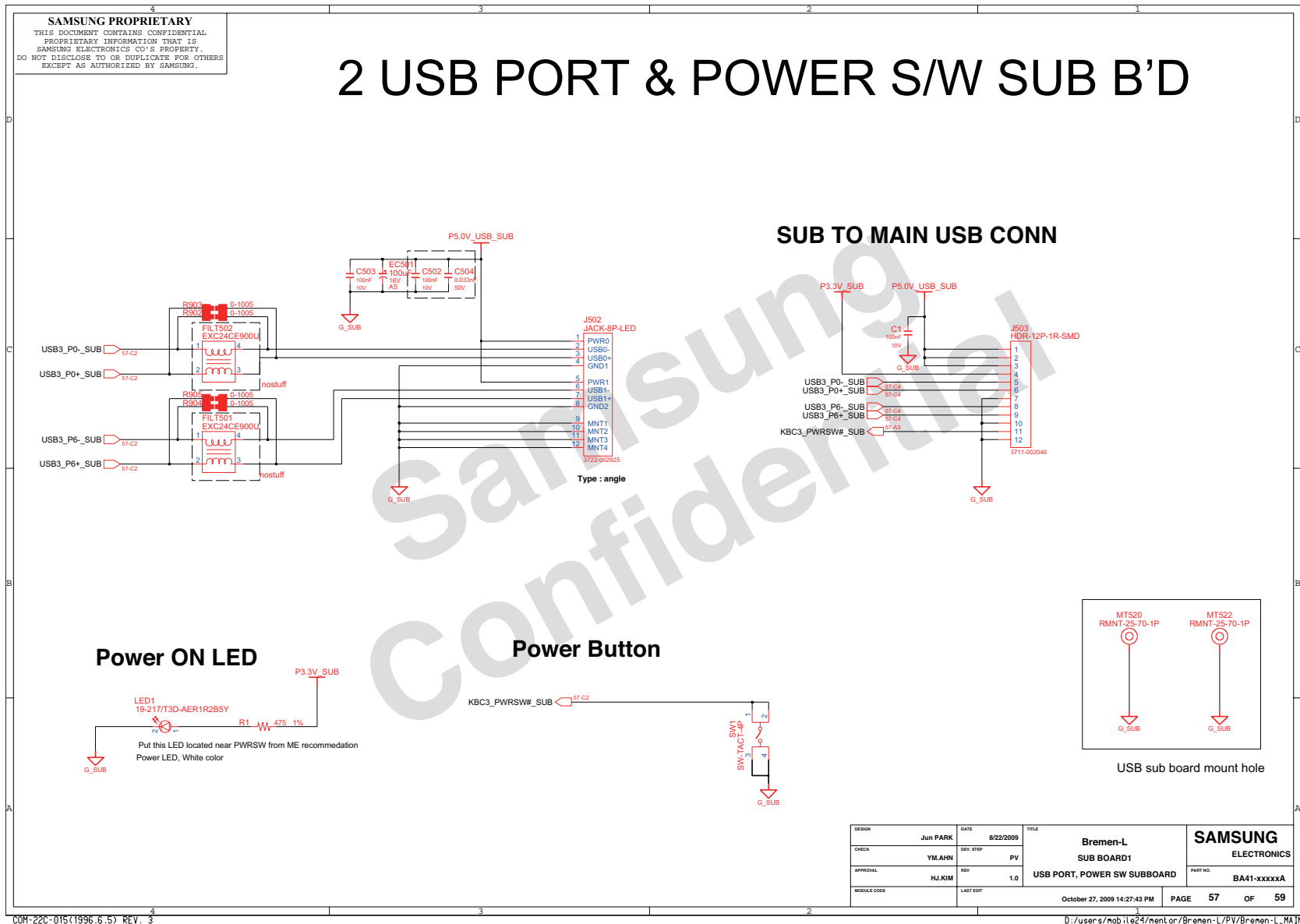


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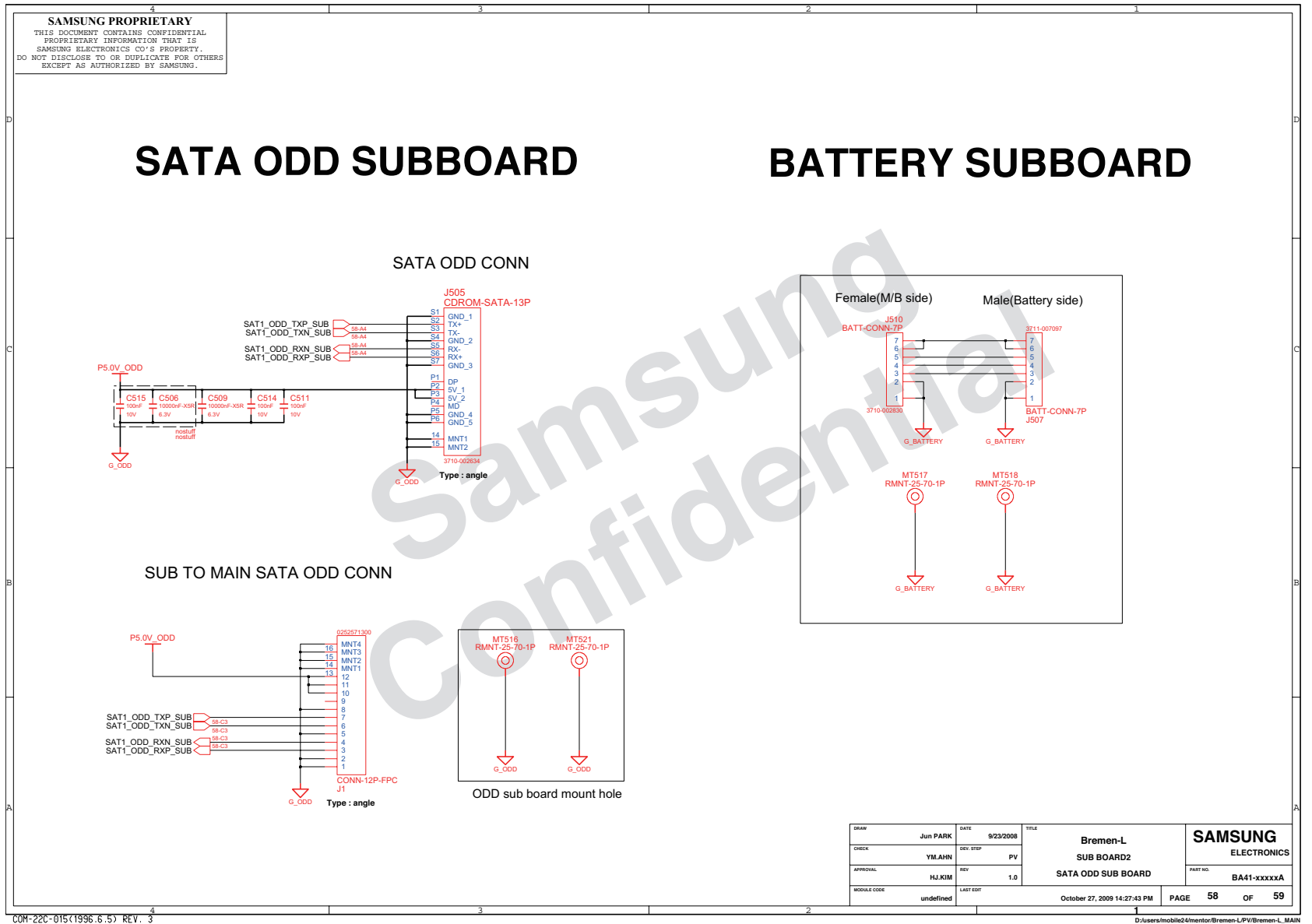




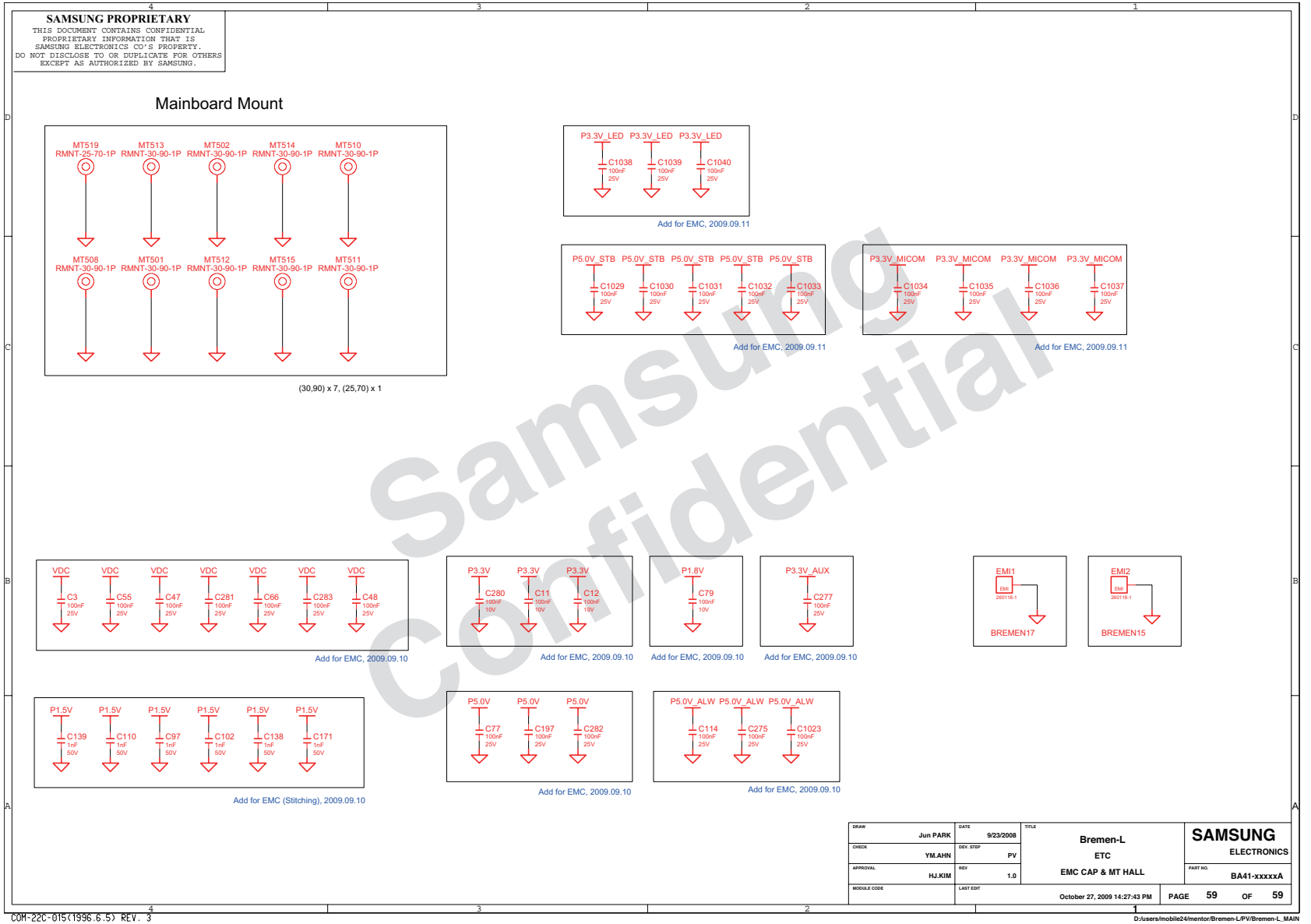
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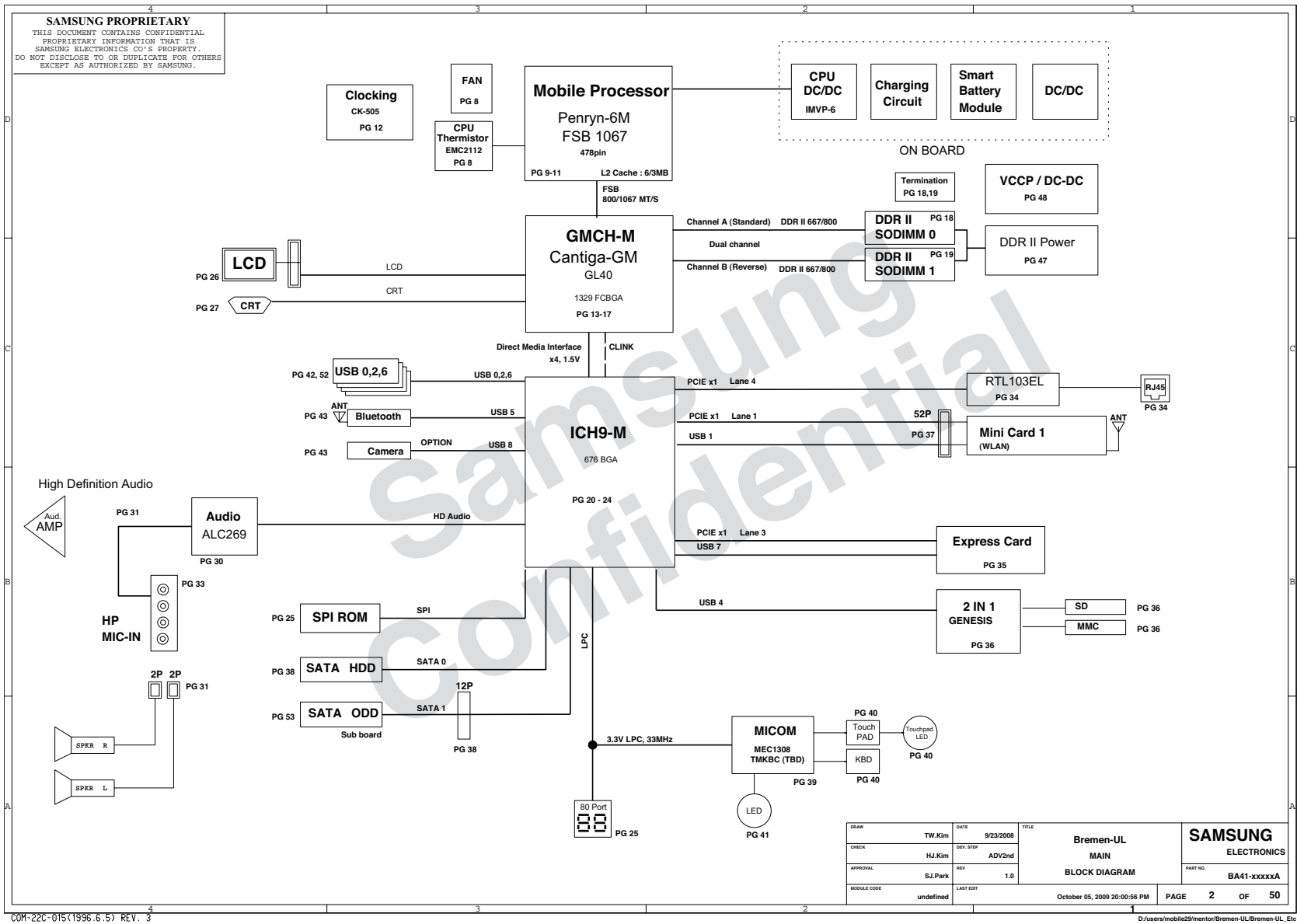
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CPU : Intel Penryn Chip Set : Intel Cantiga & ICH9M Remarks : Montevina Platform																						
<div>Model Name : Bremen-UL PBA Name : MAIN PCB Code : GCE : BA41-01177A NAN : BA41-01178A HAN : BA41-01179A Dev. Step : PV Revision : 1.0 T.R. Date : 2009.10.19</div>																						
Design	CHECK	APPROVAL																				
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices			
Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails	
VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	0	NC
1	SYSTEM PORT 1	1	Mini Card 1 (WLAN)
2	SYSTEM PORT 2	2	NC
3	NC	3	LOM
4	NC	4	Mini Card 2 (ROBSON or DVB-T)
5	Bluetooth	5	NC
6	Mini PCI Express 2		
7	Camera		
8	NC		
9	NC		

(This table will be update.)

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	RealTek 88E8057

LCD Pannel Detect (TBD)		
Devices	Resolution	PANNEL_DETECT_0

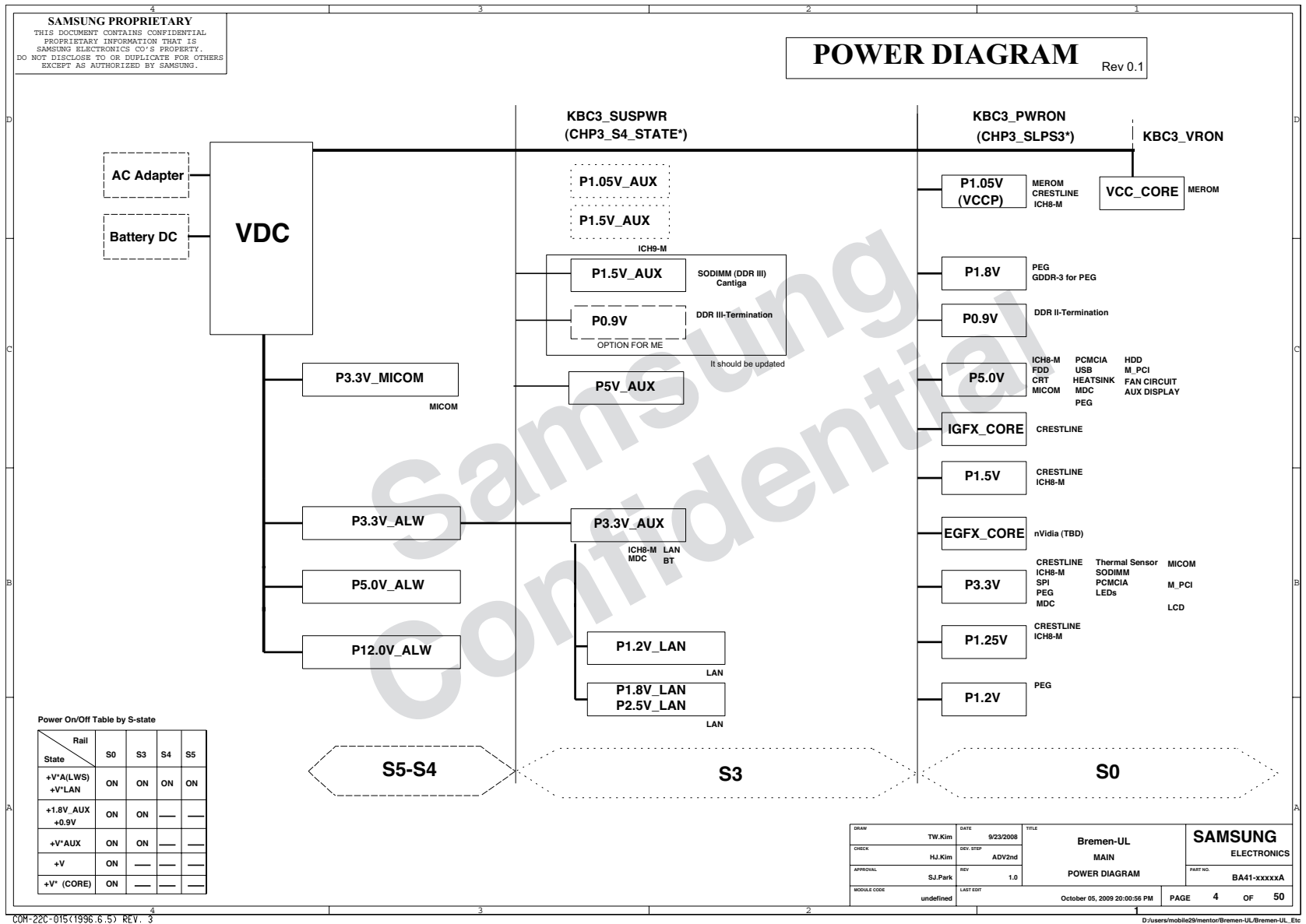
I ² C / SMB Address			
Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

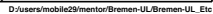
REVISION HISTORY

See rev notes for more information.

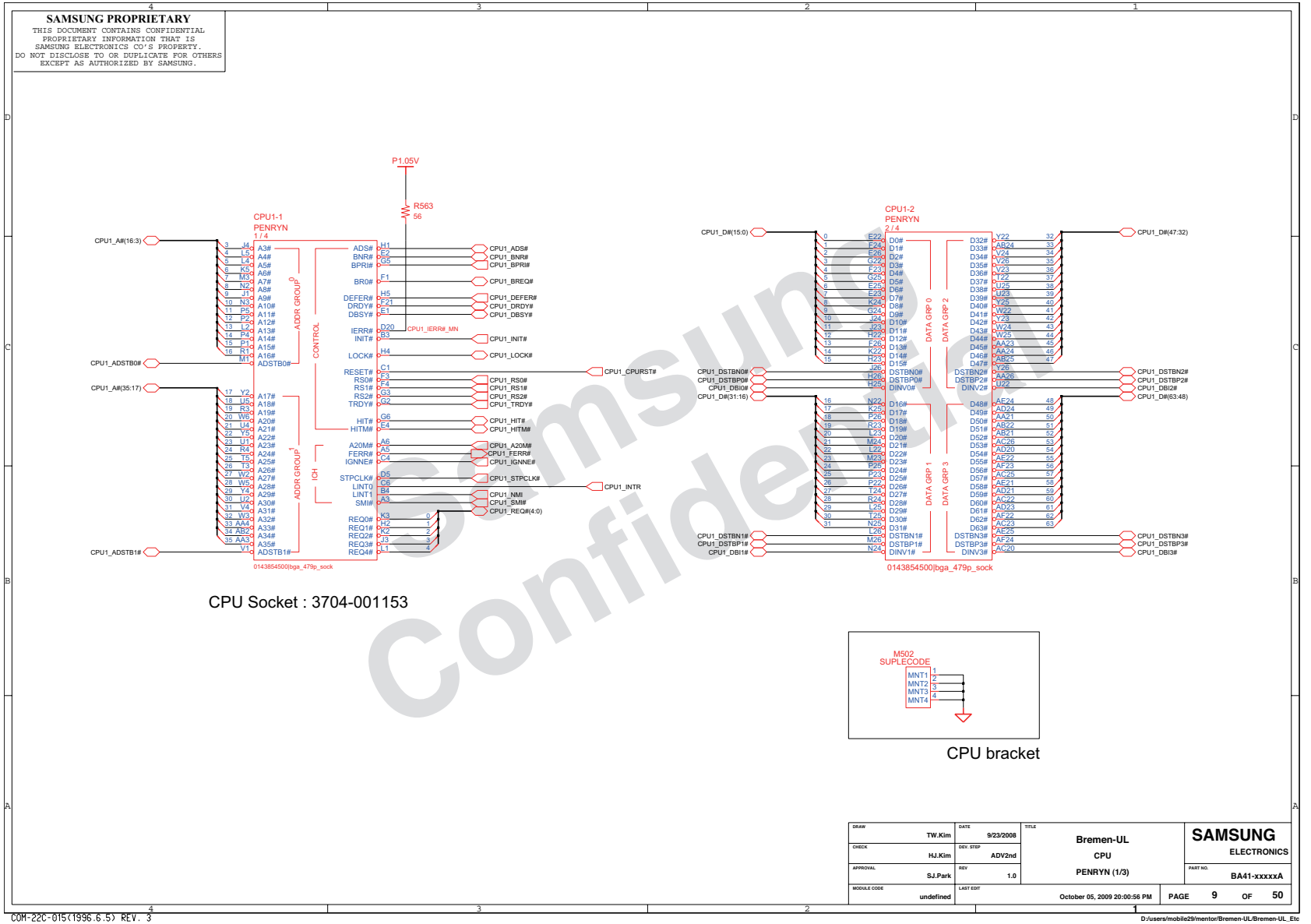
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CHECK	HJ.Kim	REV. STEP	ADV2nd	MAIN				
APPROVAL	S.J.Park	REV	1.0	BOARD INFO				
MODULE CODE	undefined	LAST EDIT	October 05, 2009 20:00:56 PM		PAGE	3	OF 50	

8. Block Diagram and Schematic

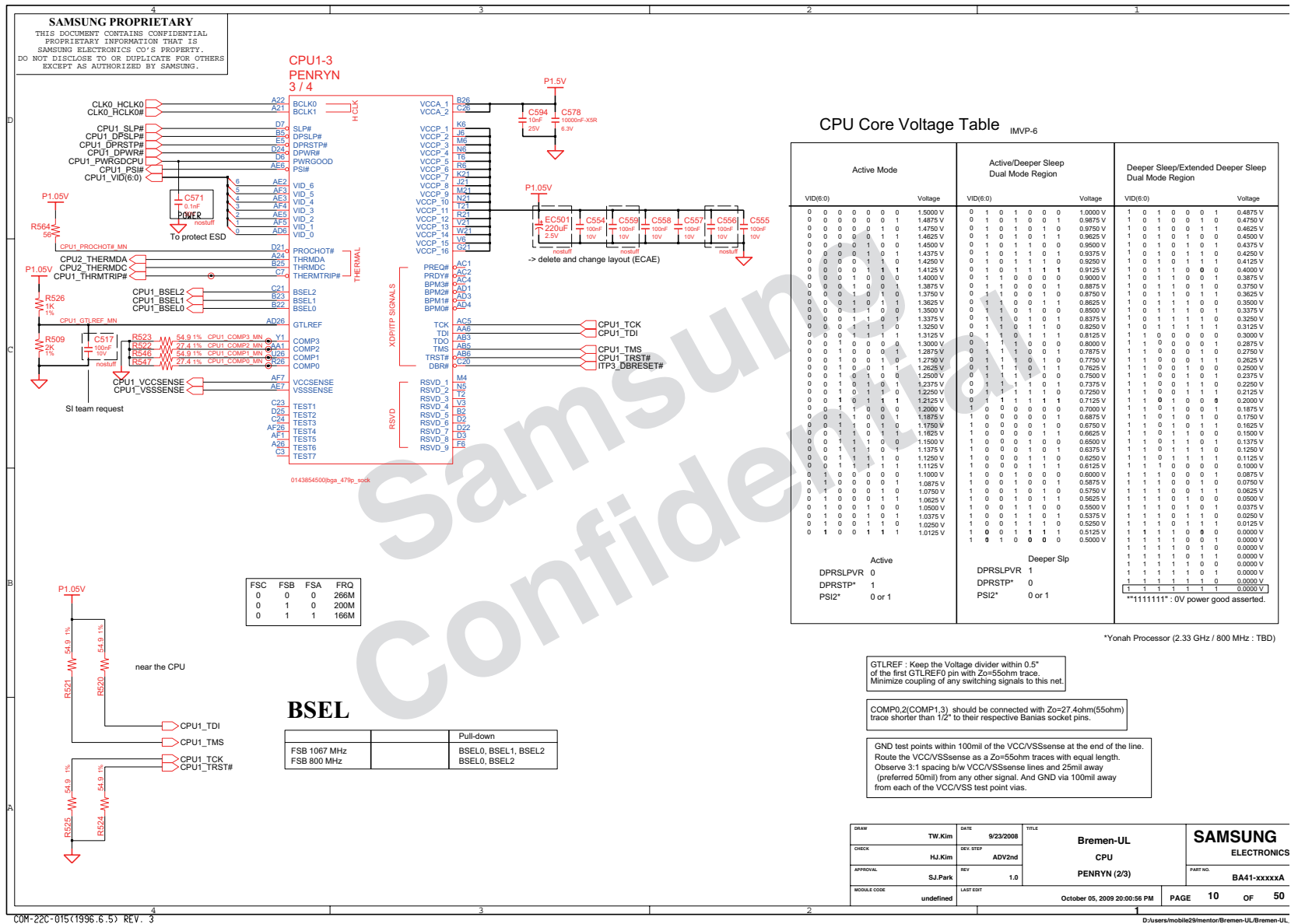




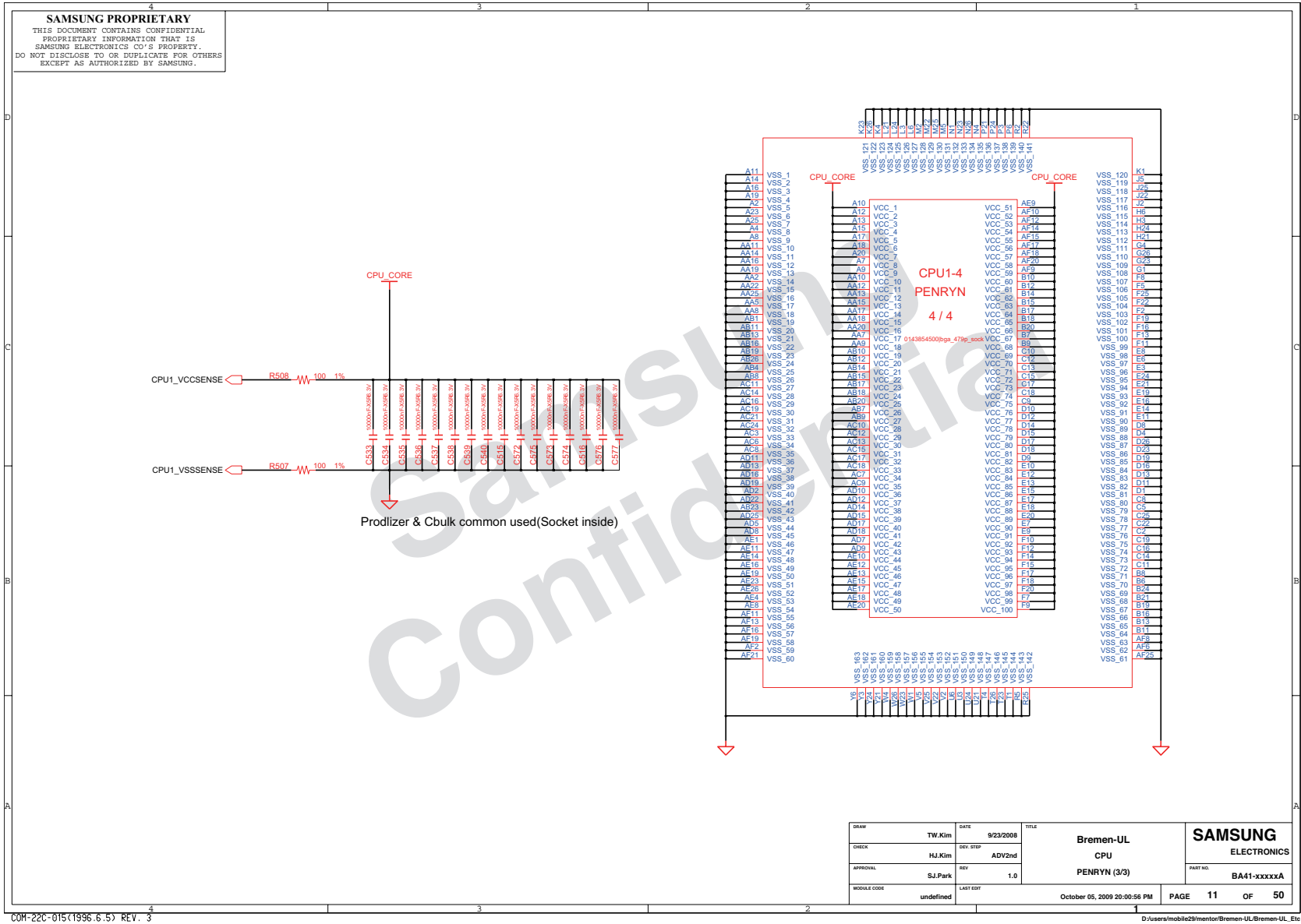
8. Block Diagram and Schematic



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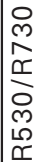




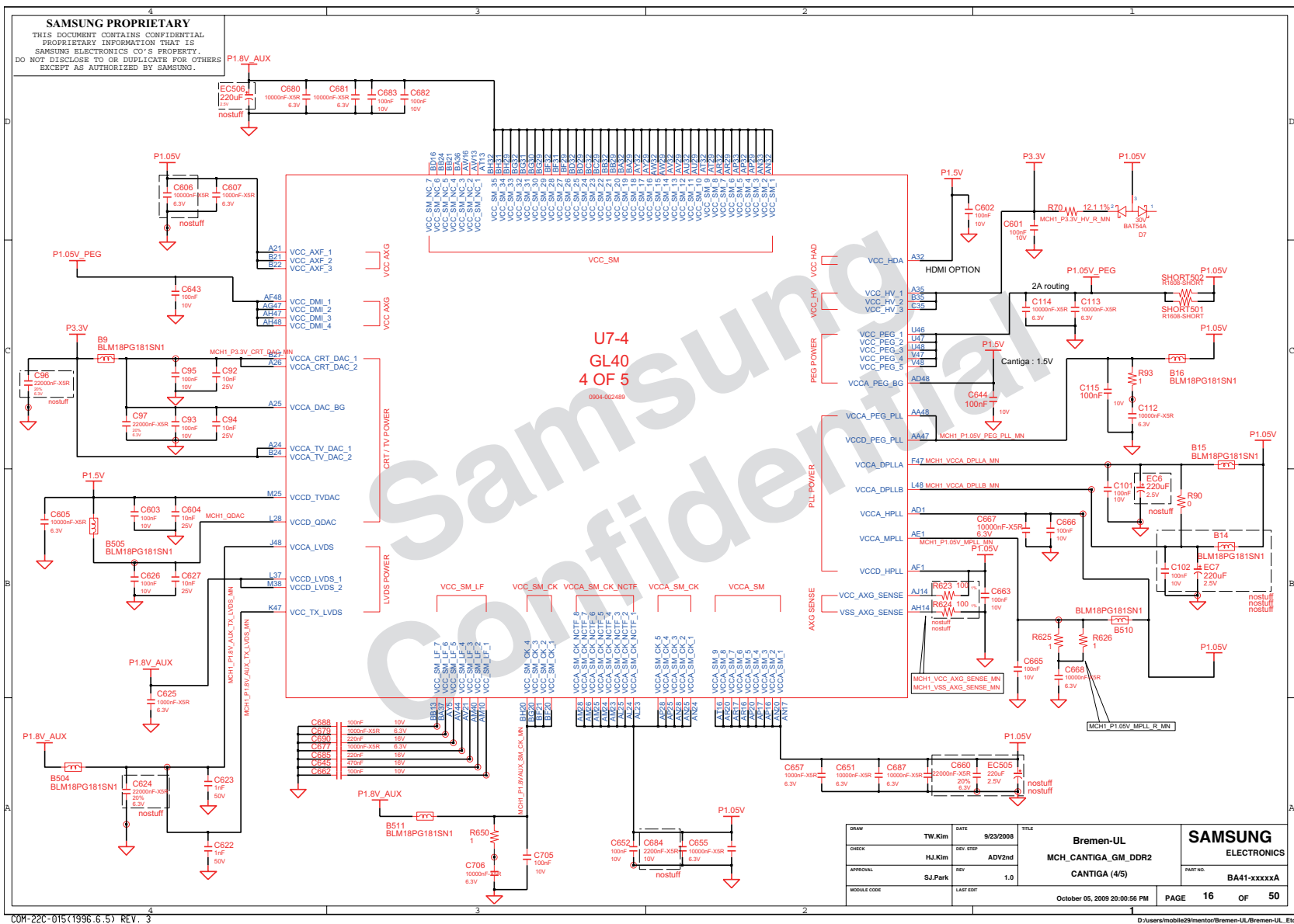


8. Block Diagram and Schematic





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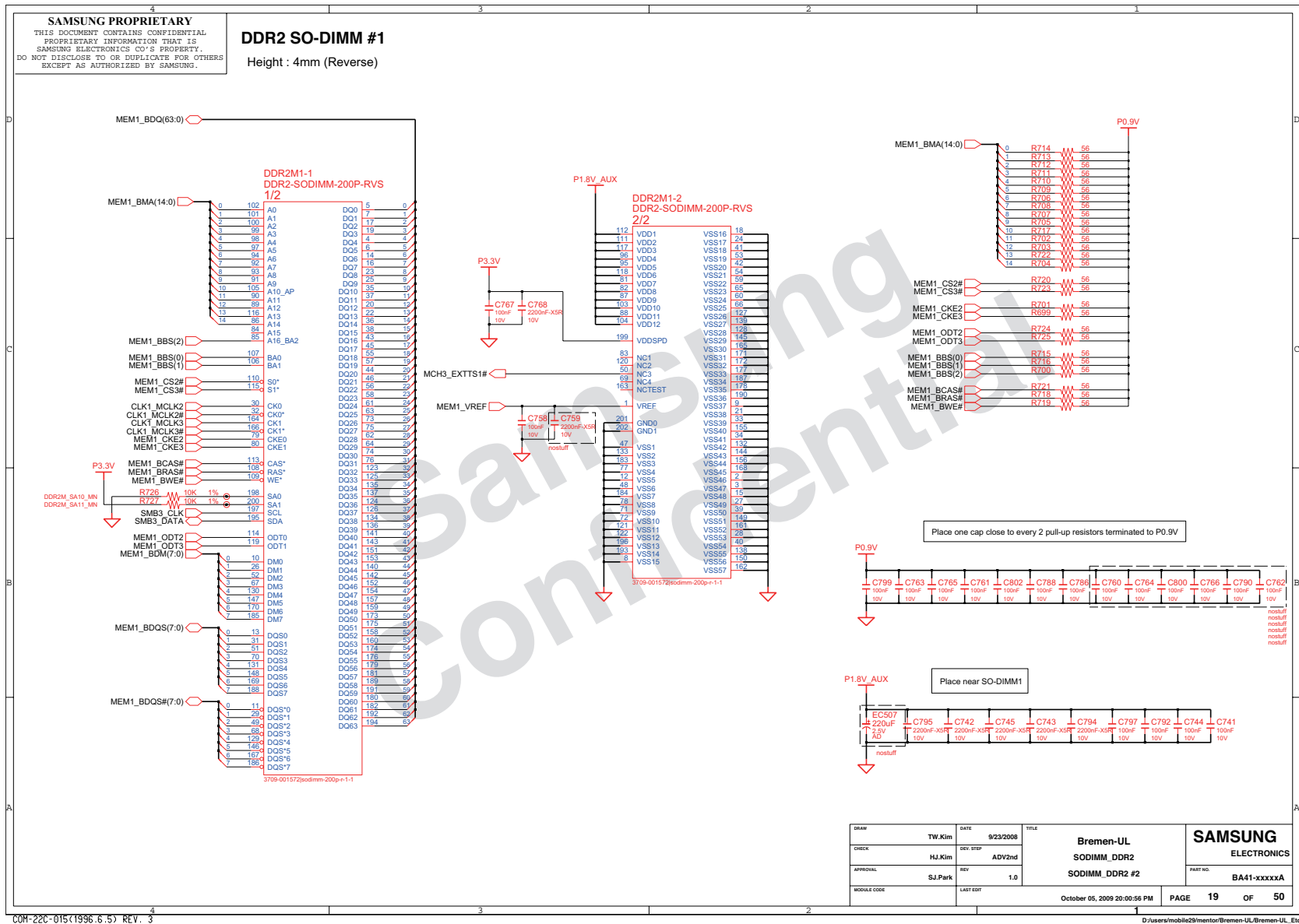


- ## 8. Block Diagram and Schematic

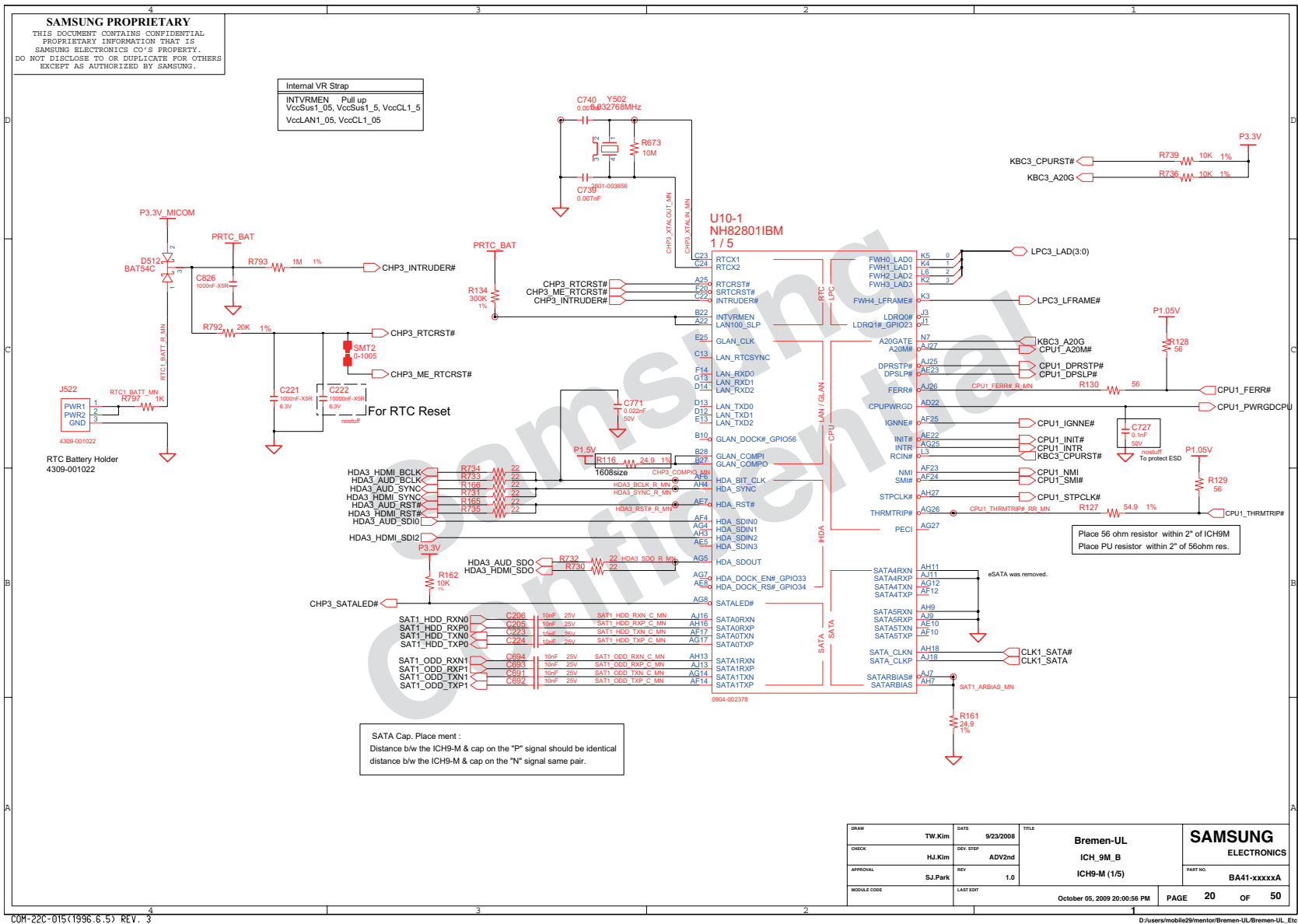




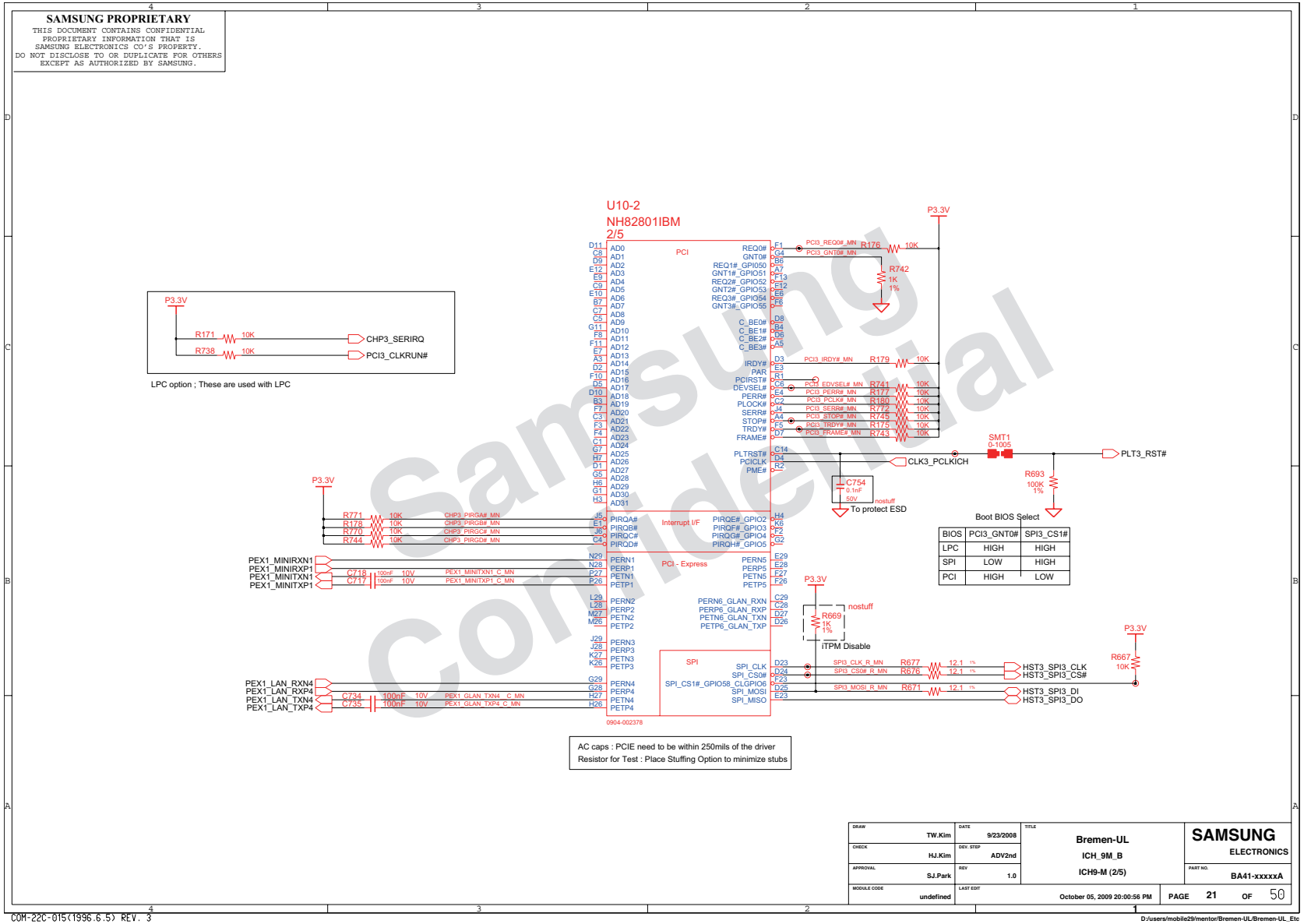
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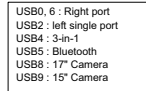


8. Block Diagram and Schematic

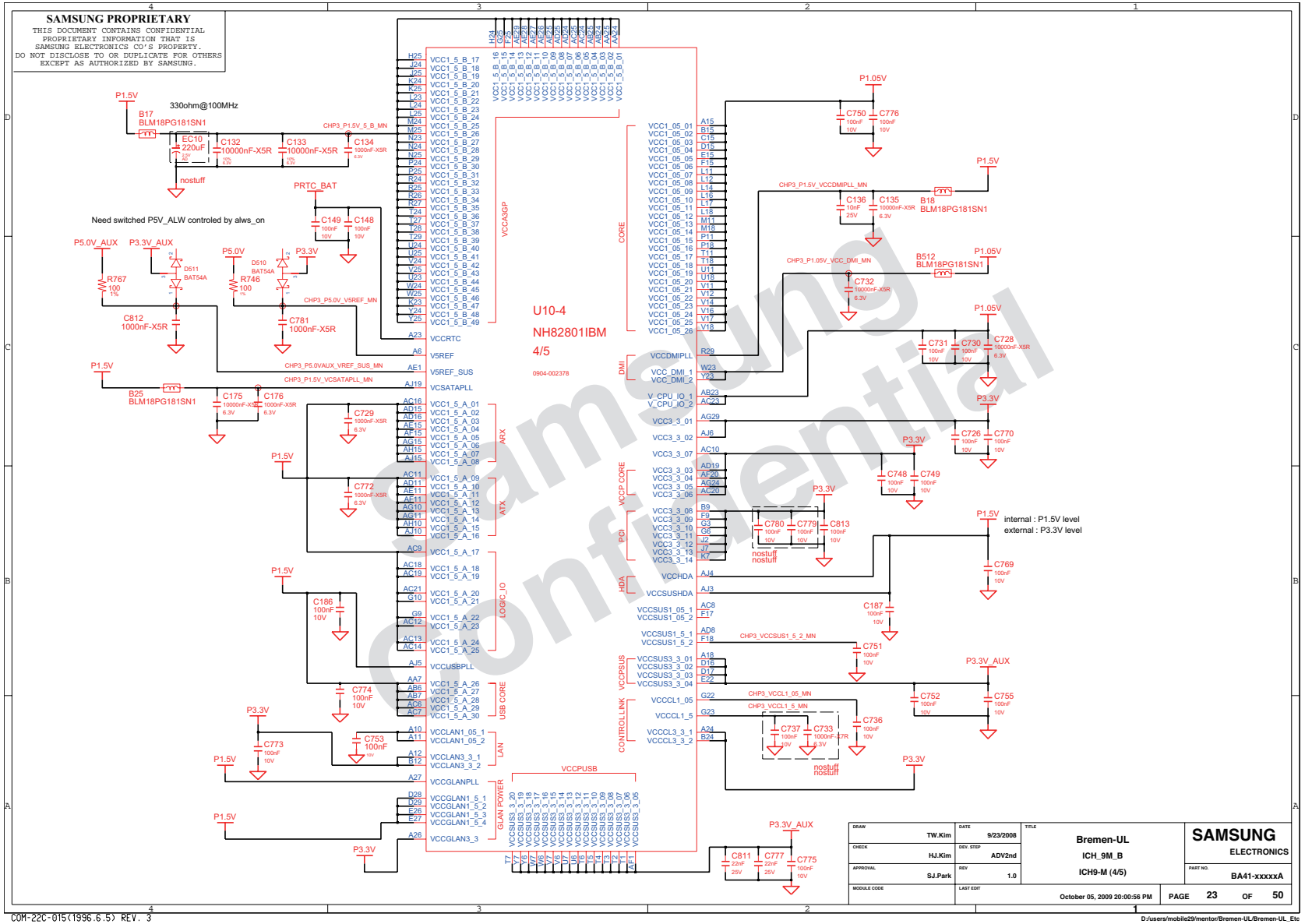


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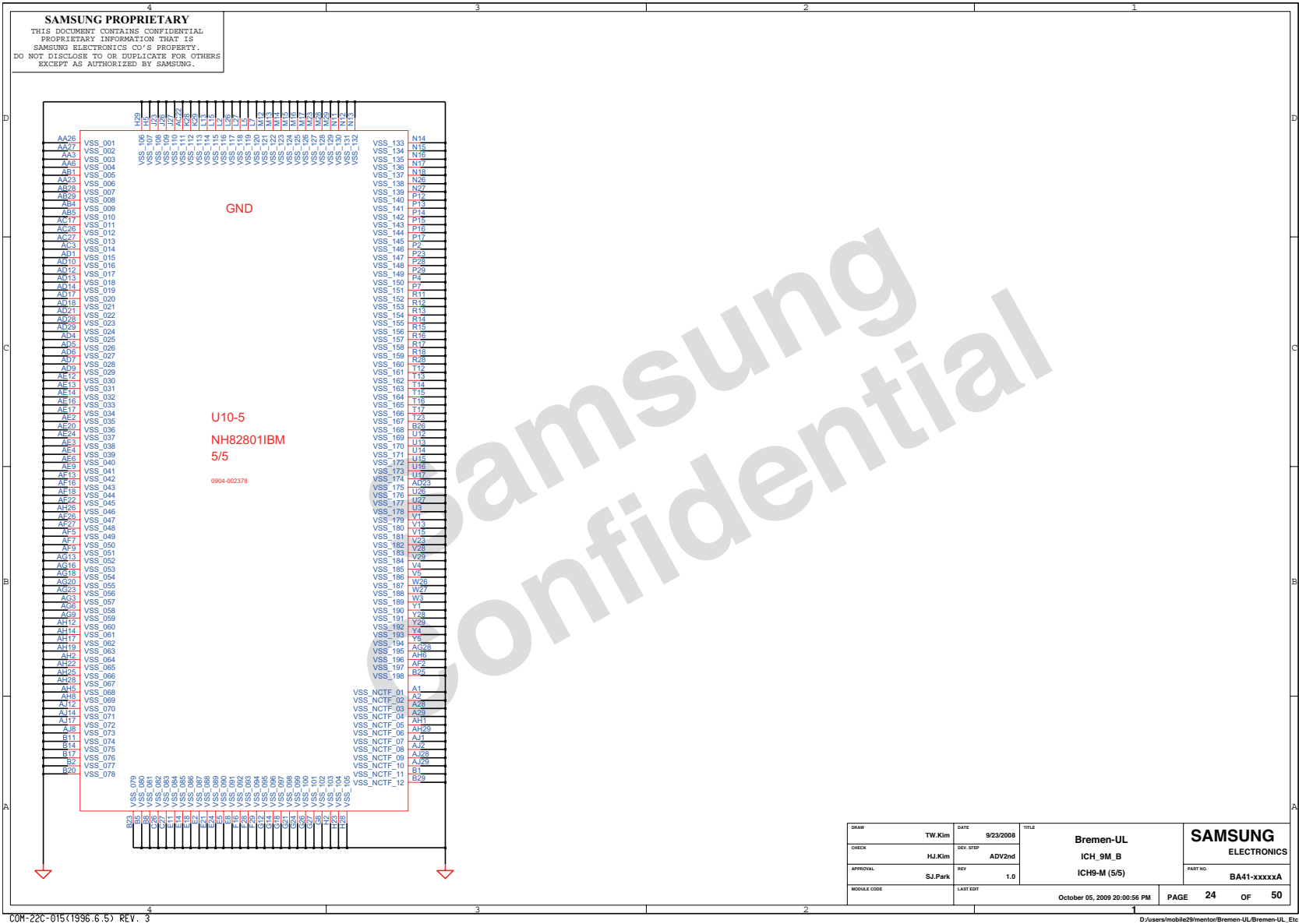




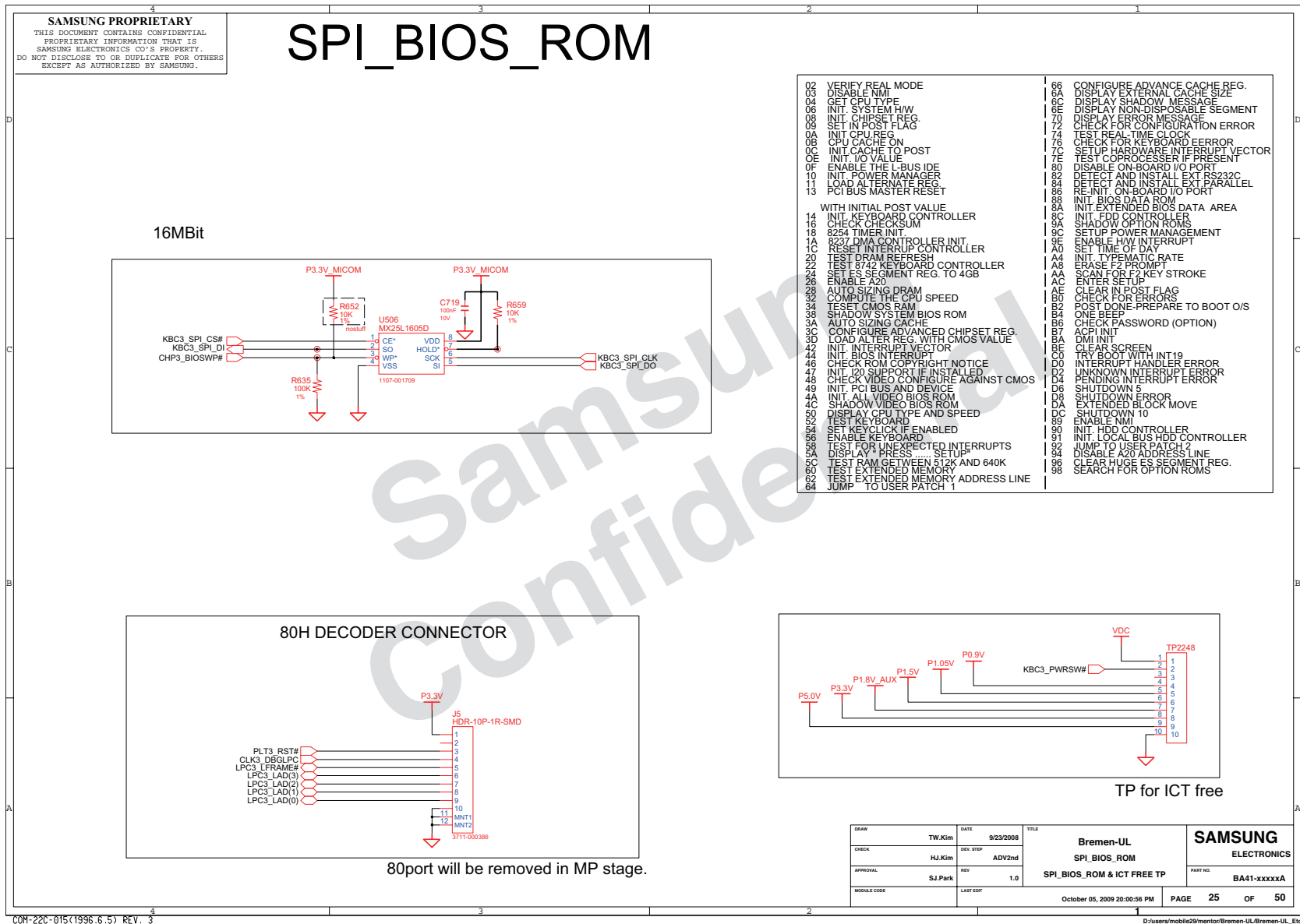
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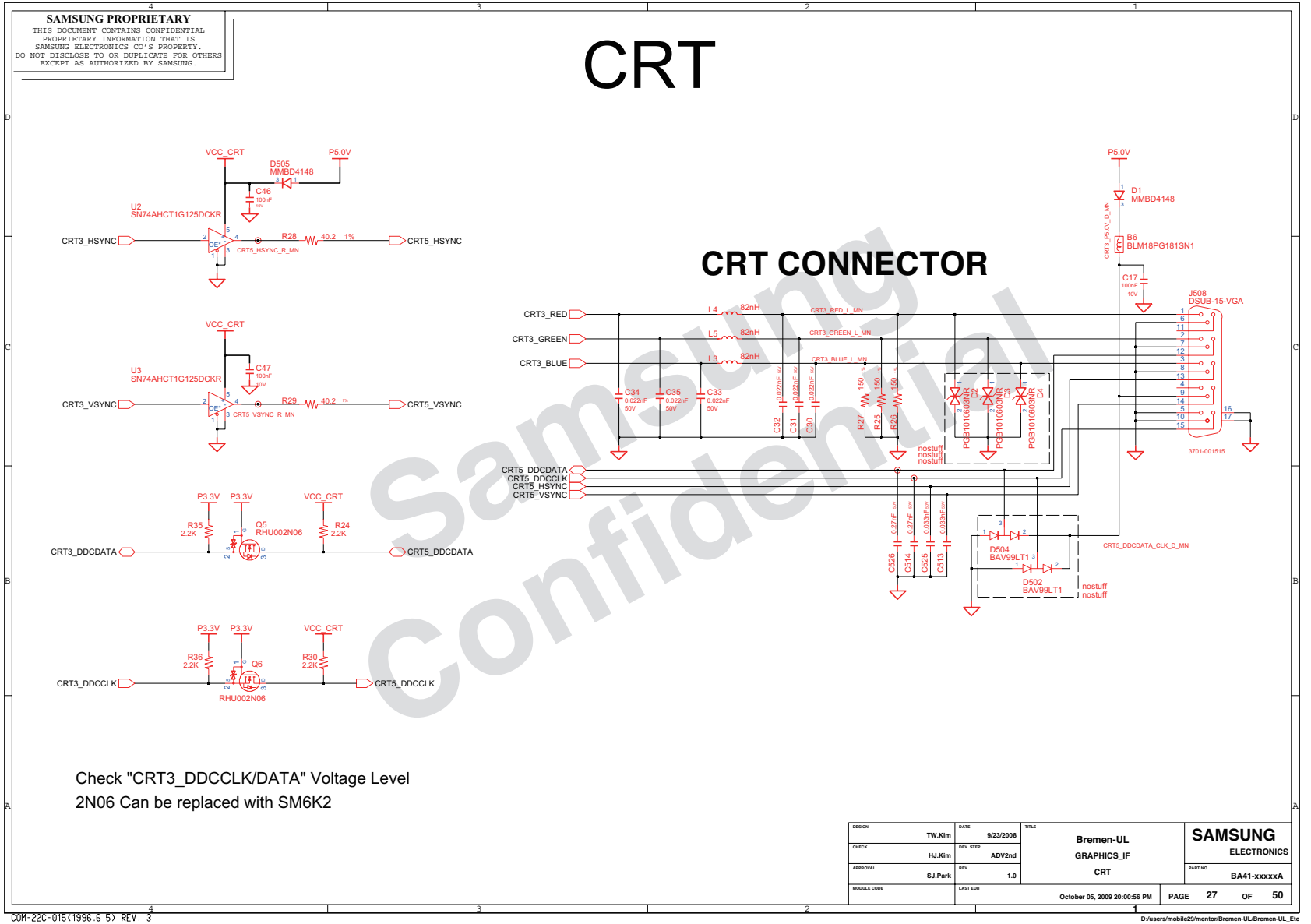


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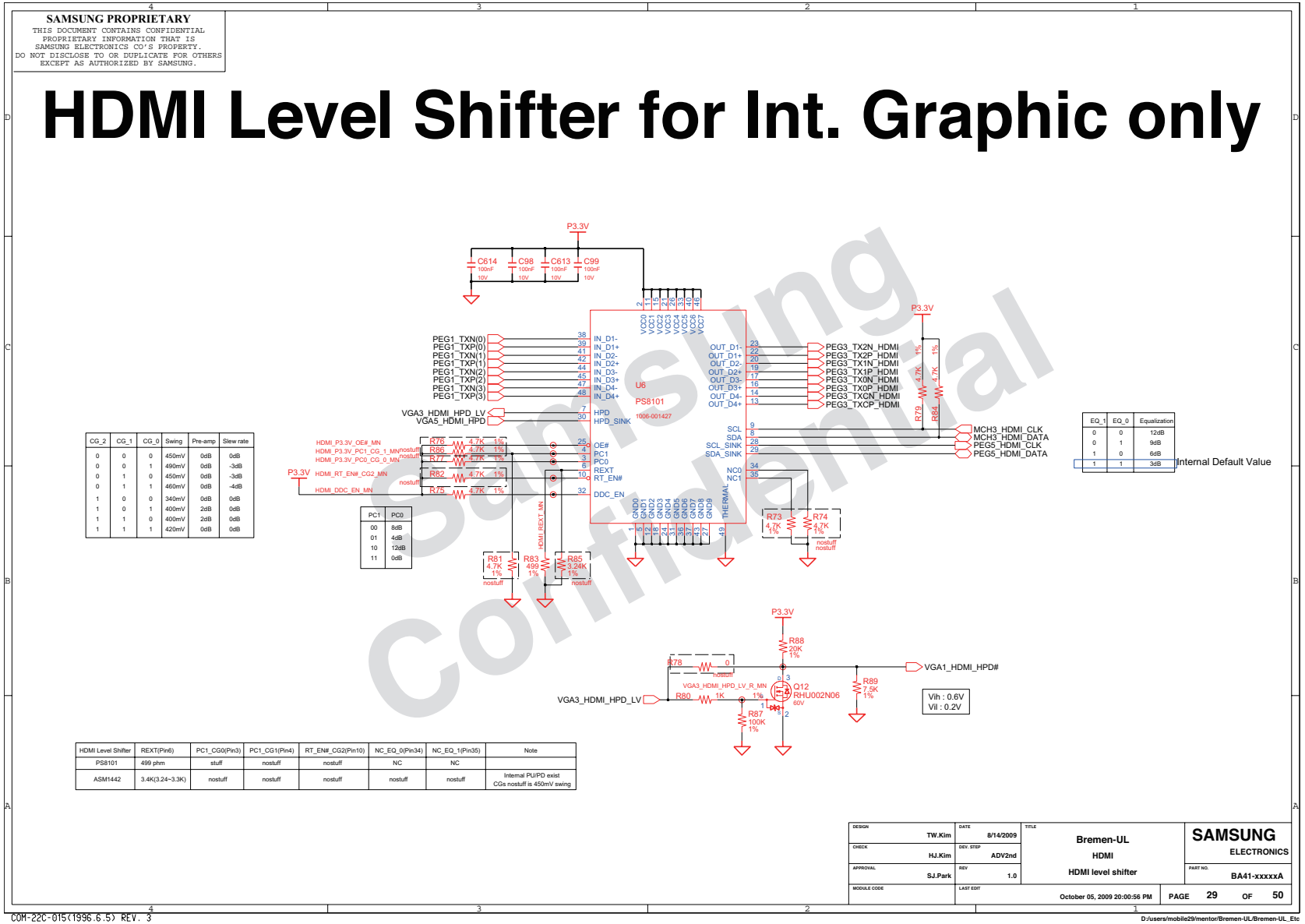


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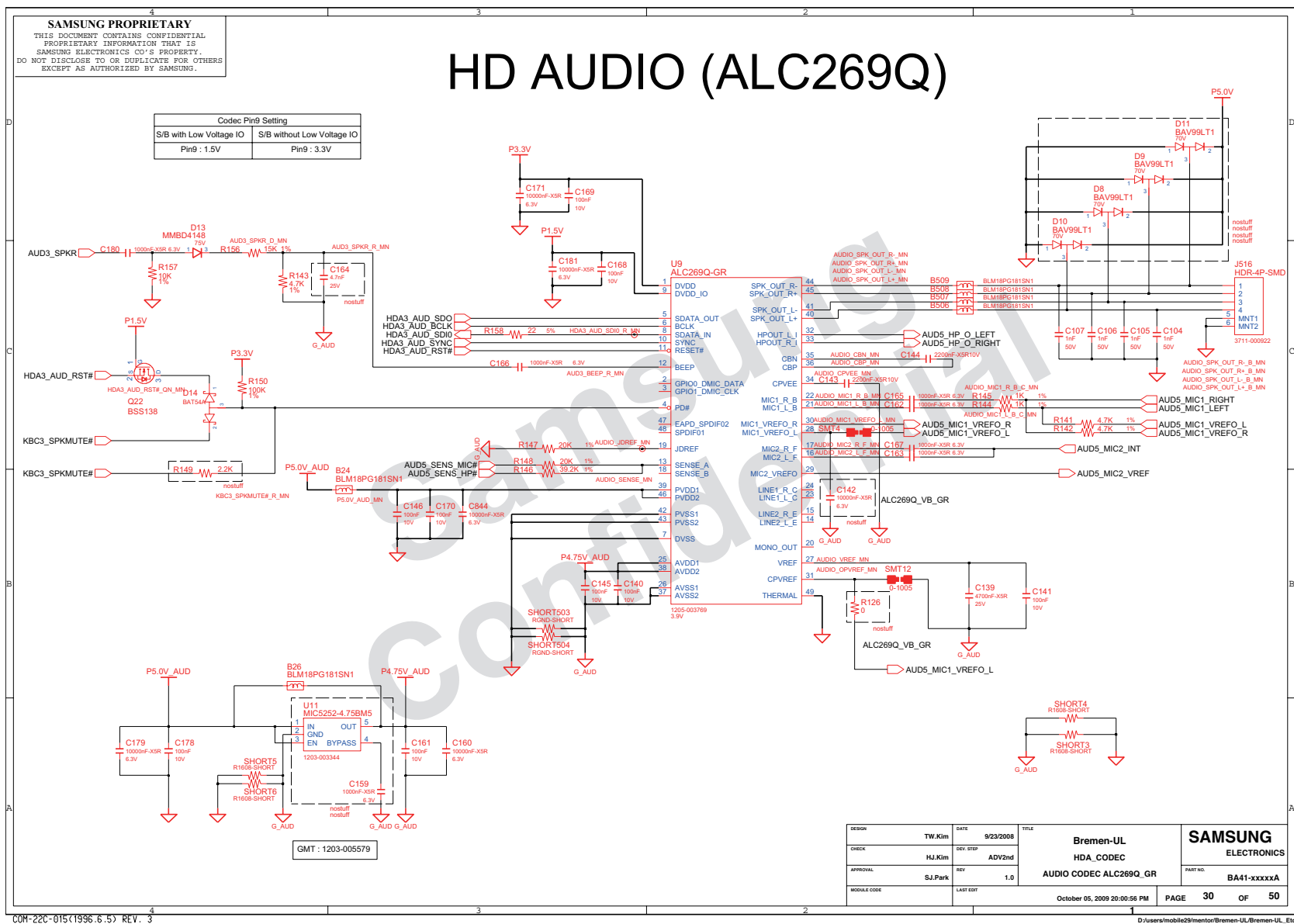




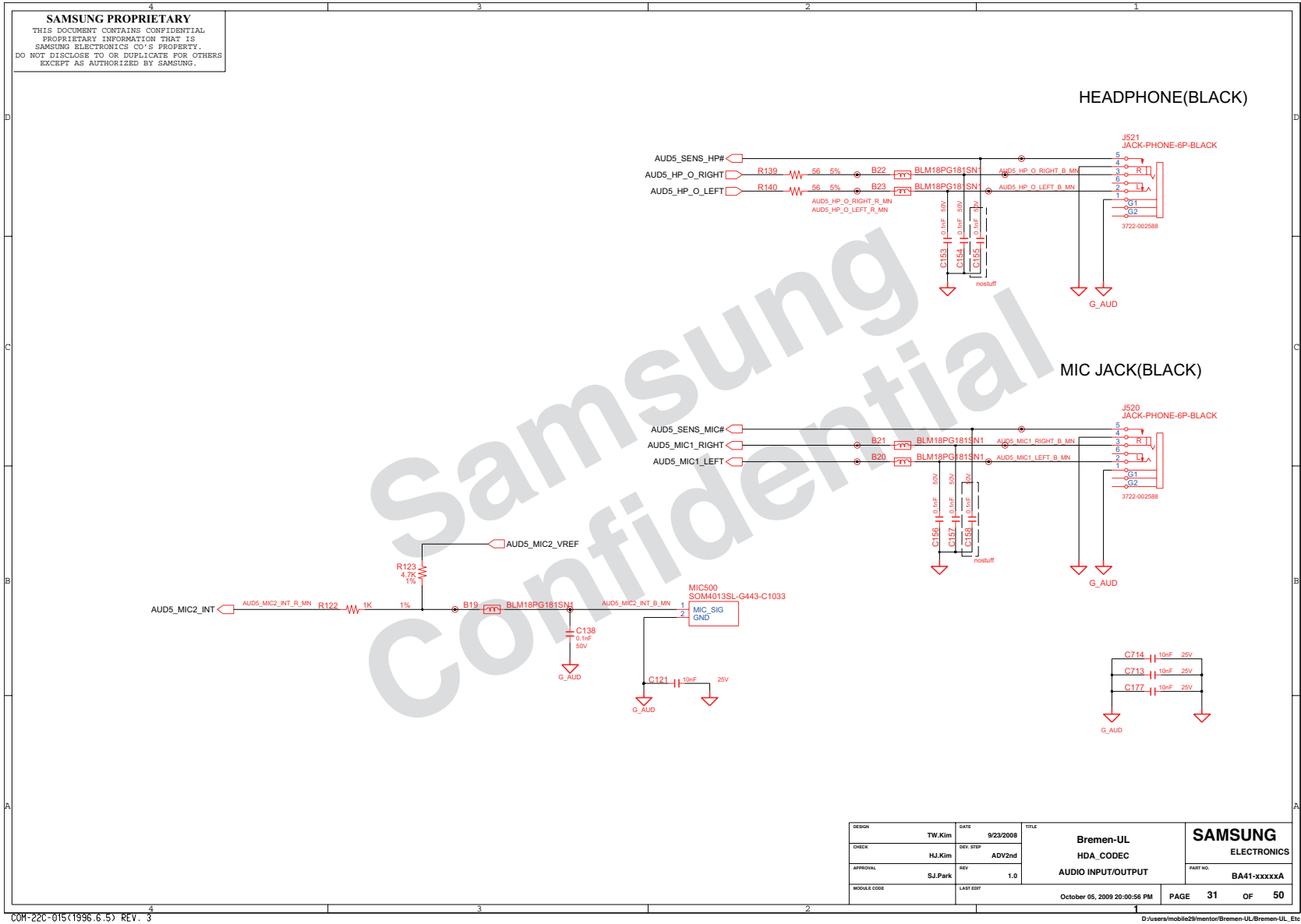
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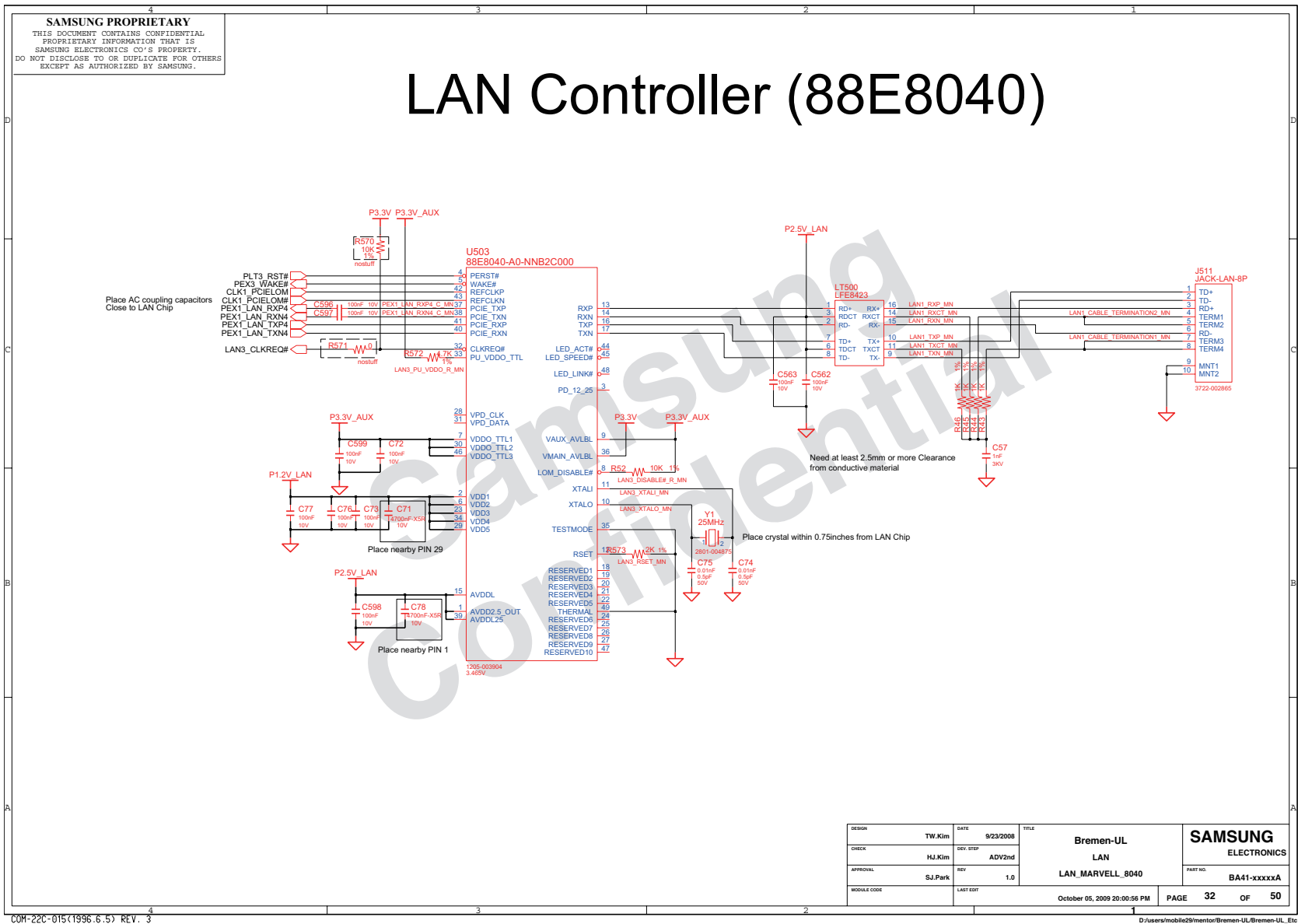
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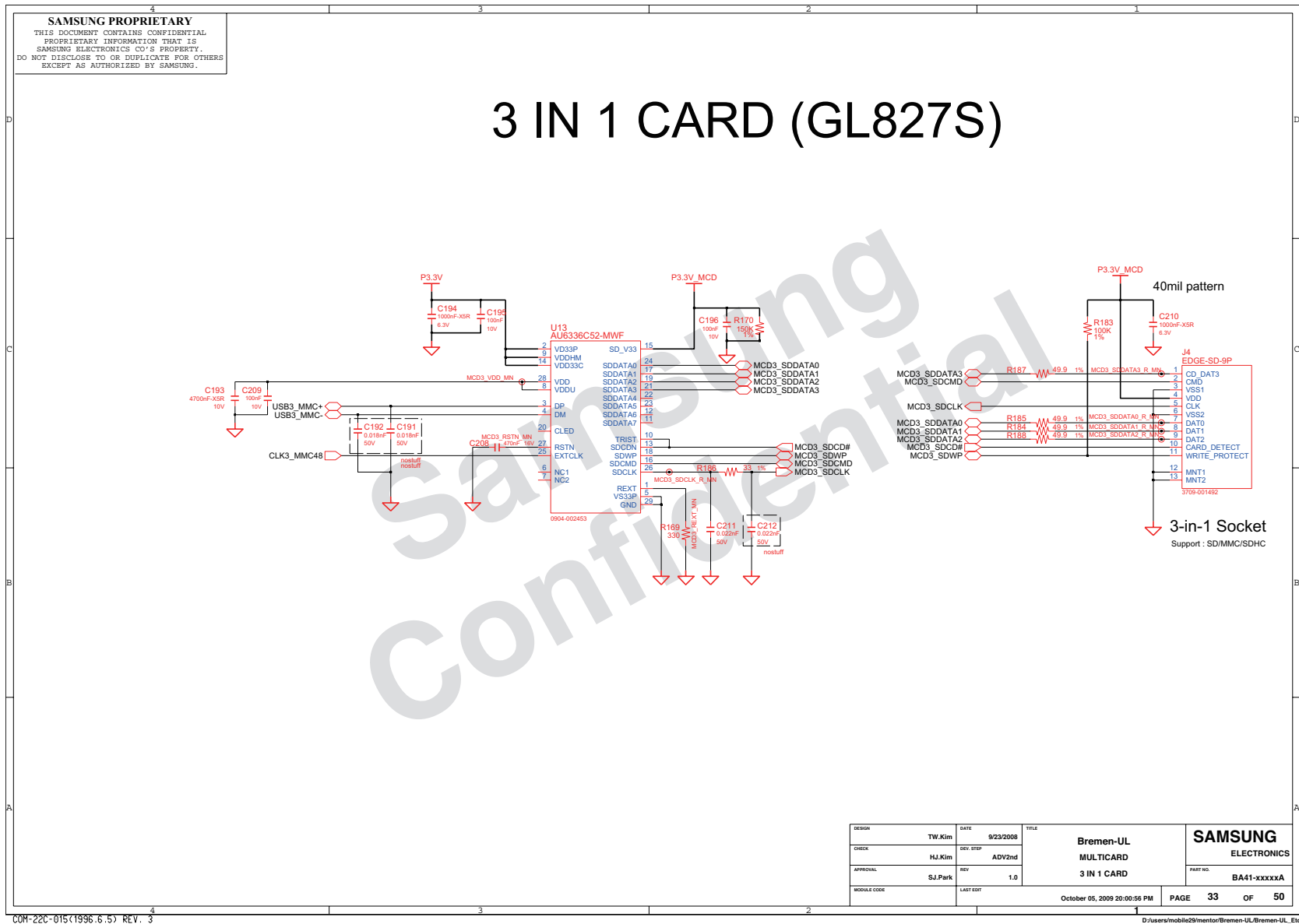
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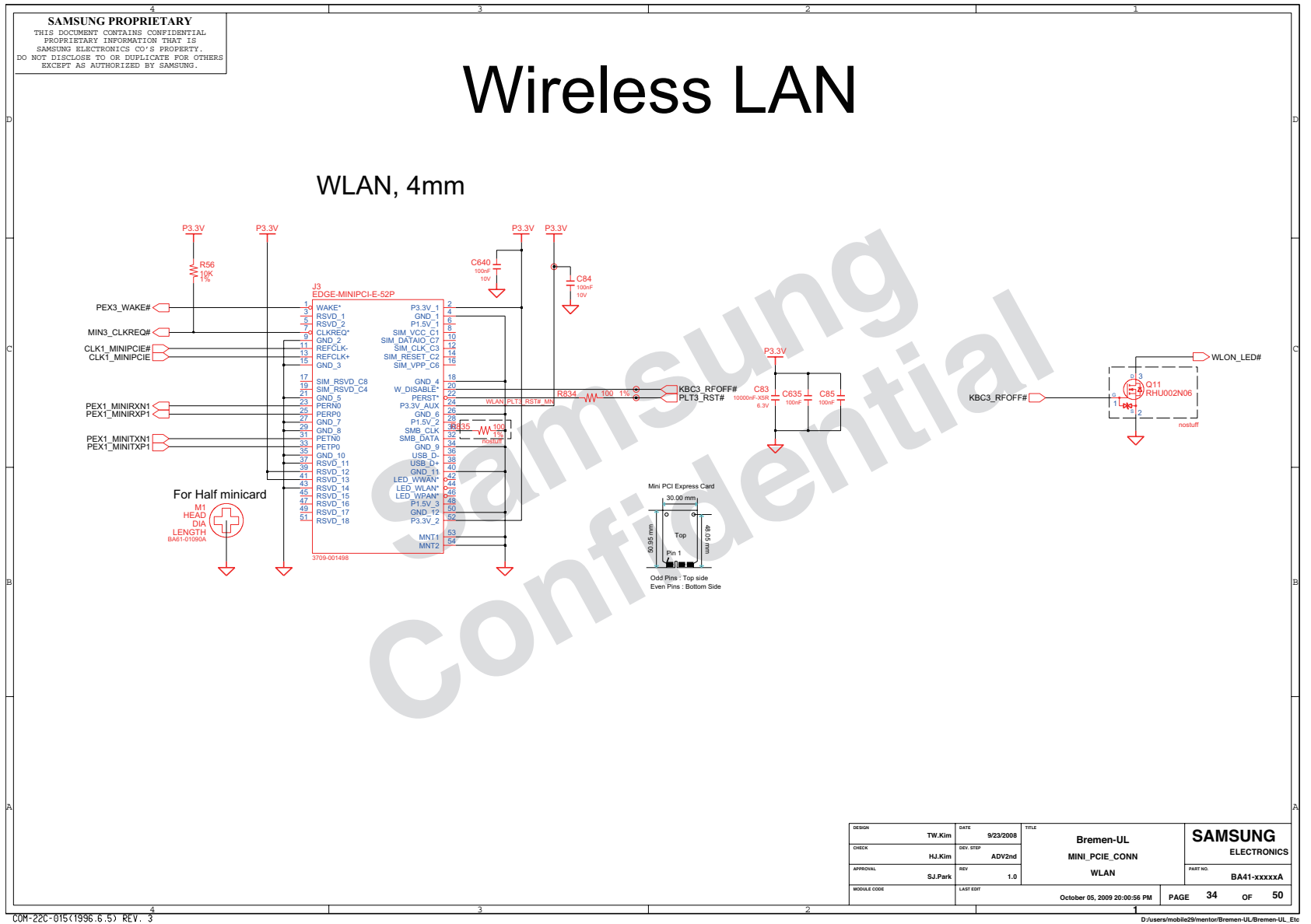
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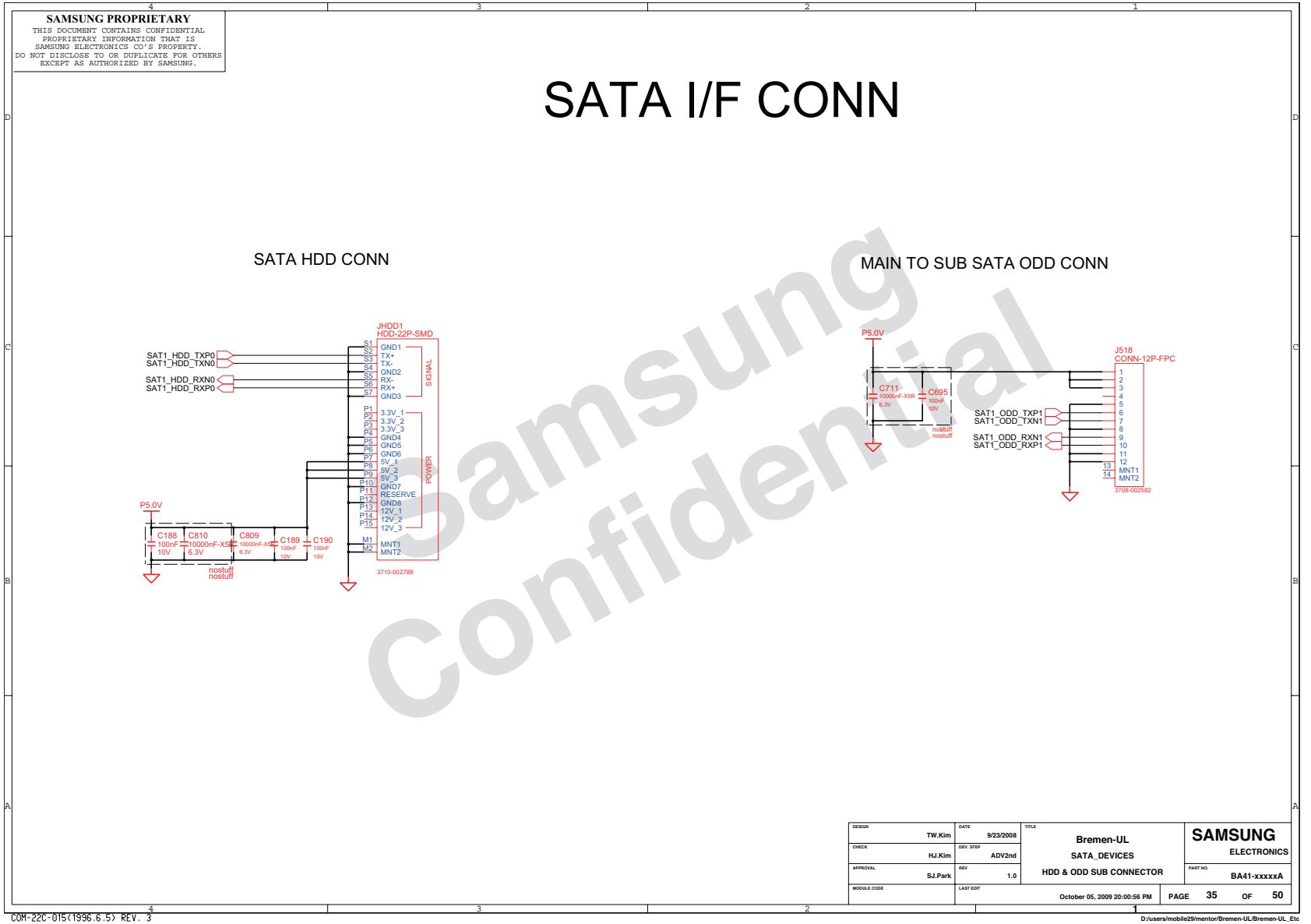
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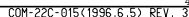
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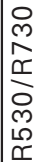


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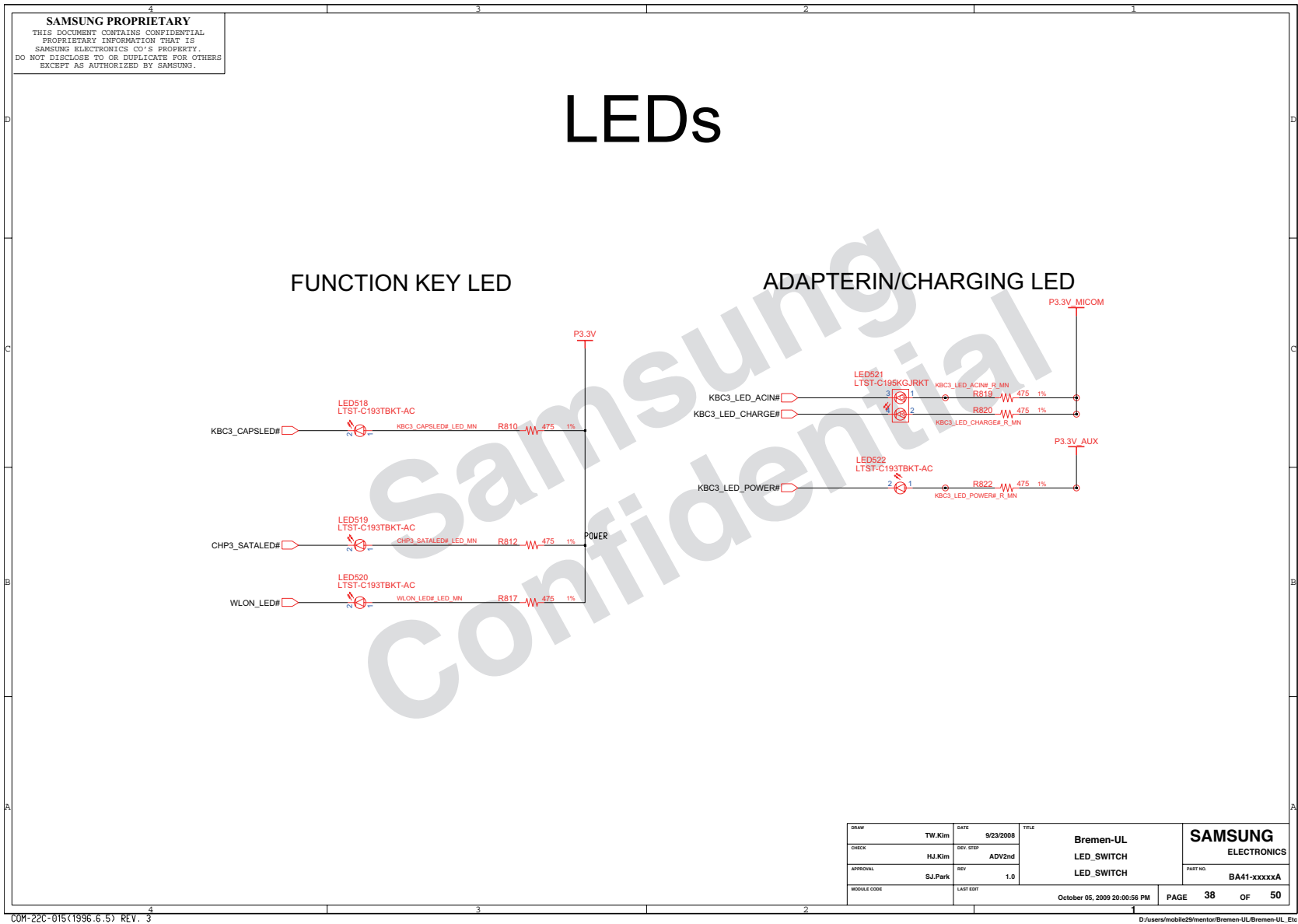


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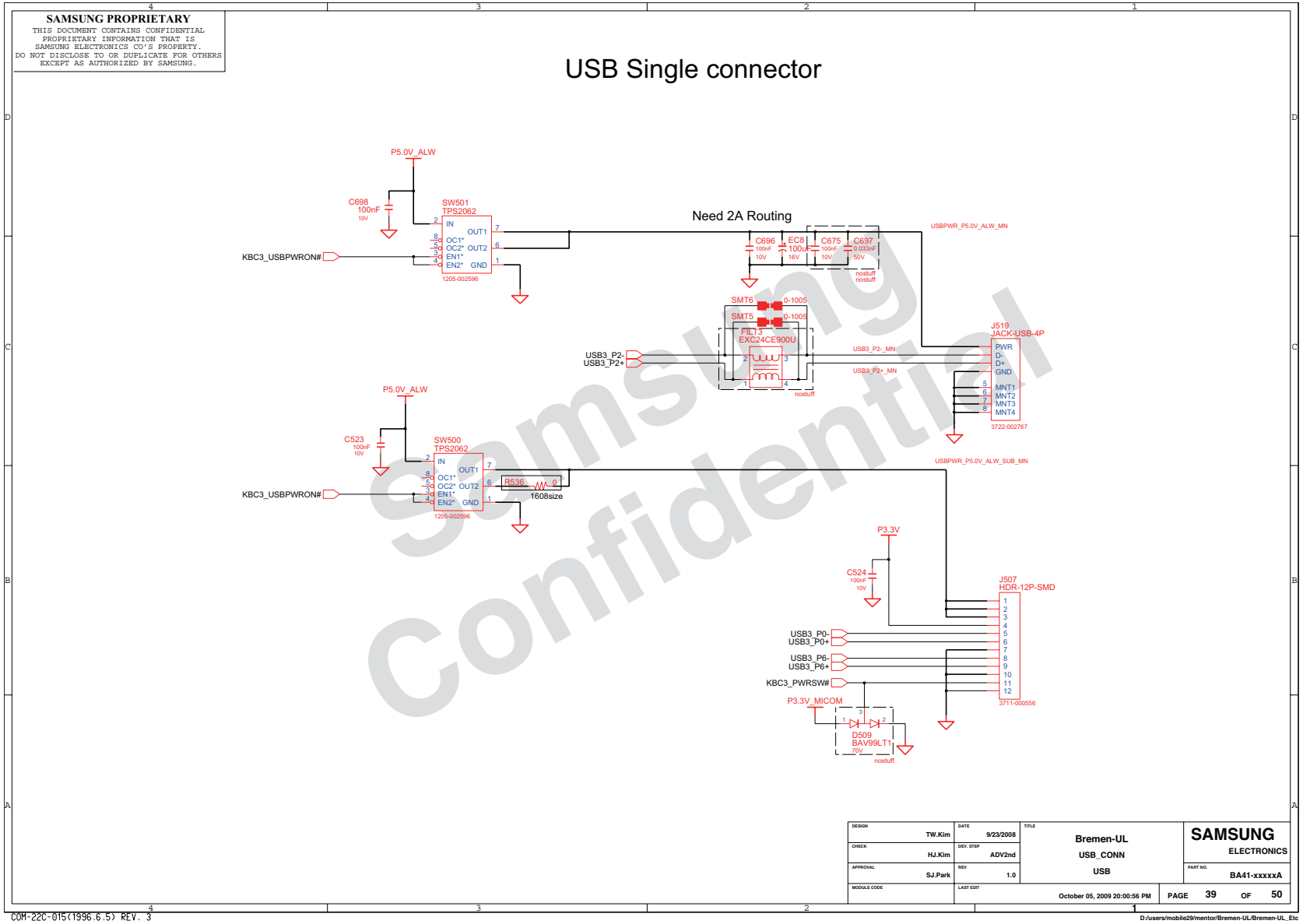




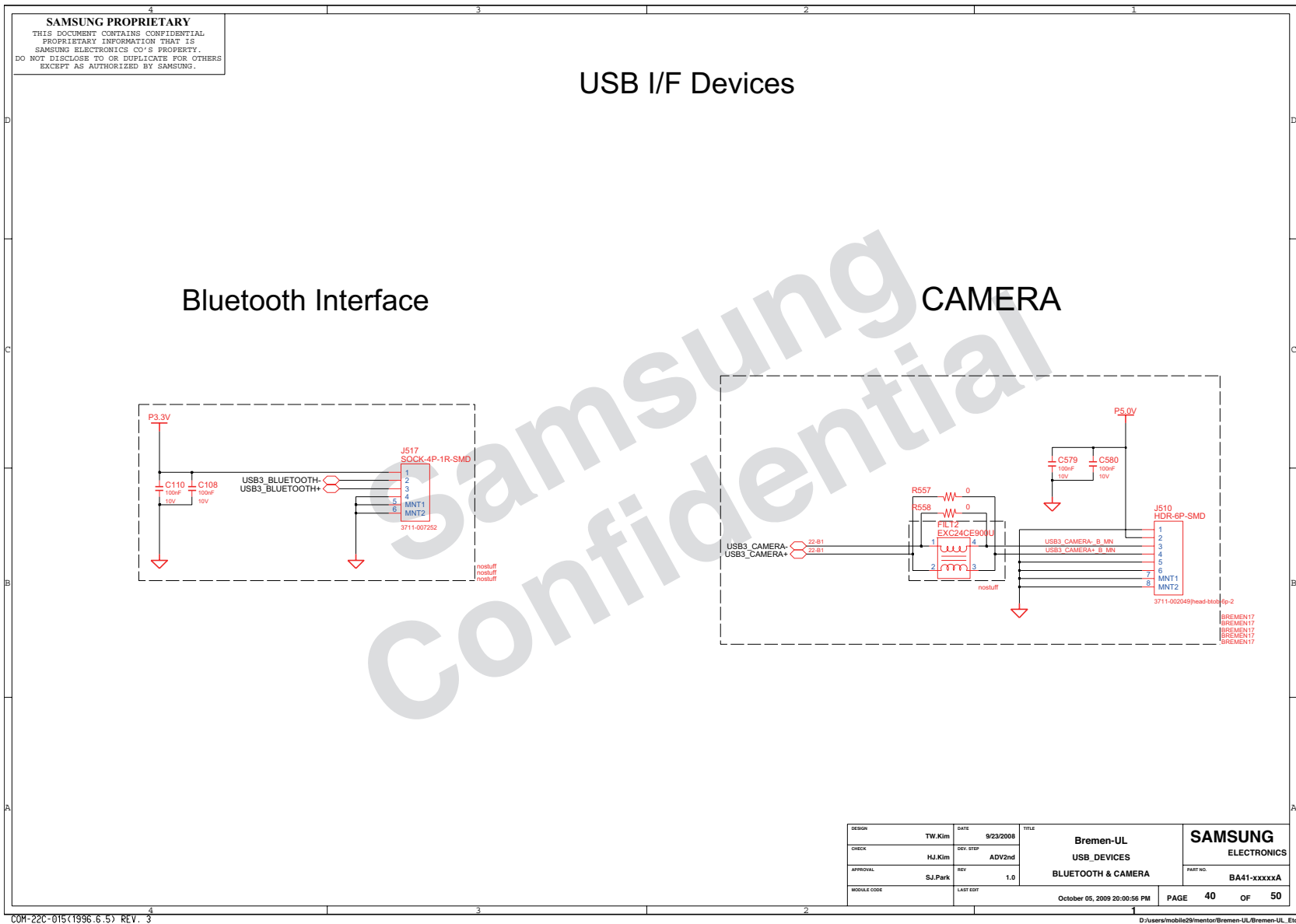
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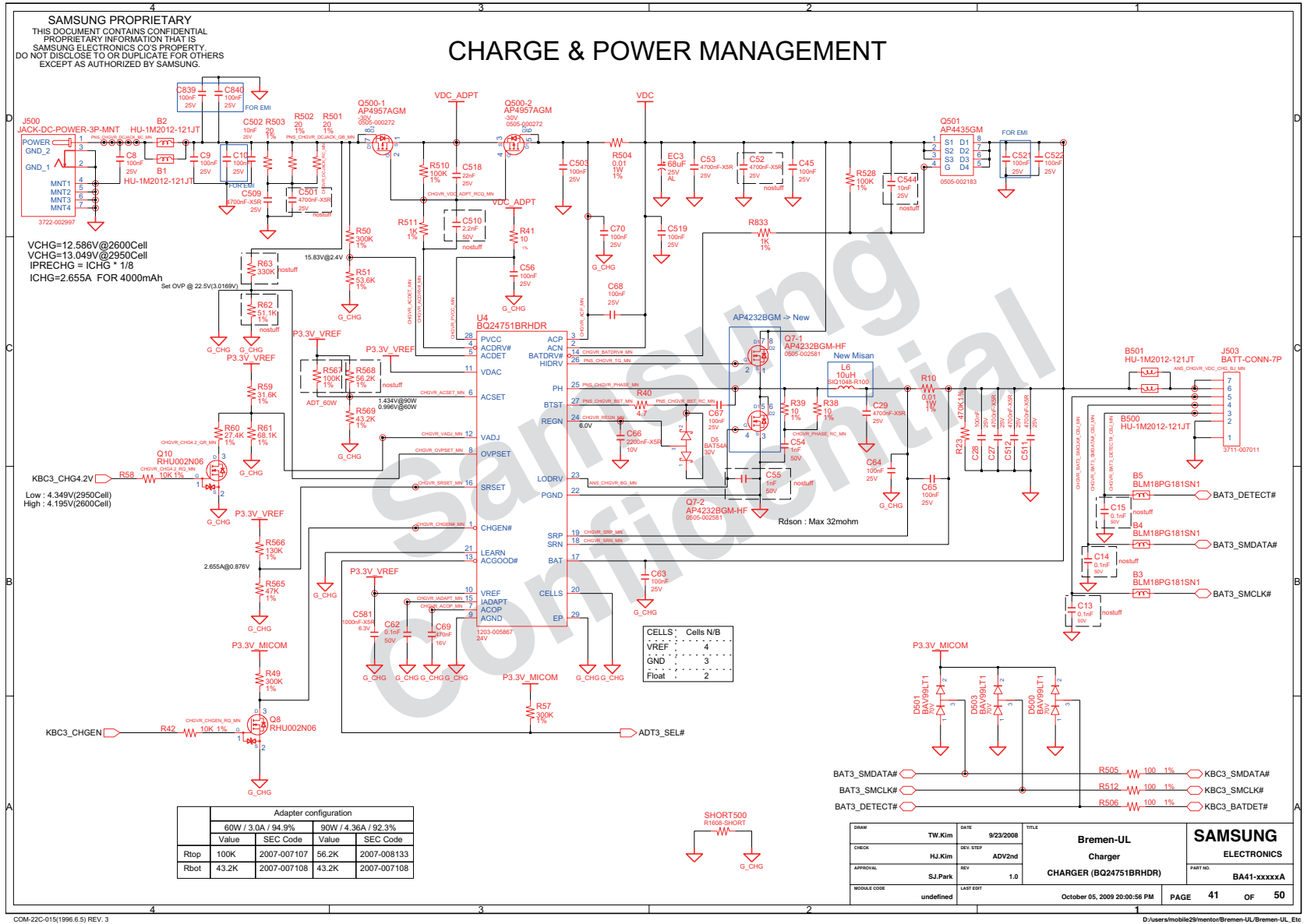
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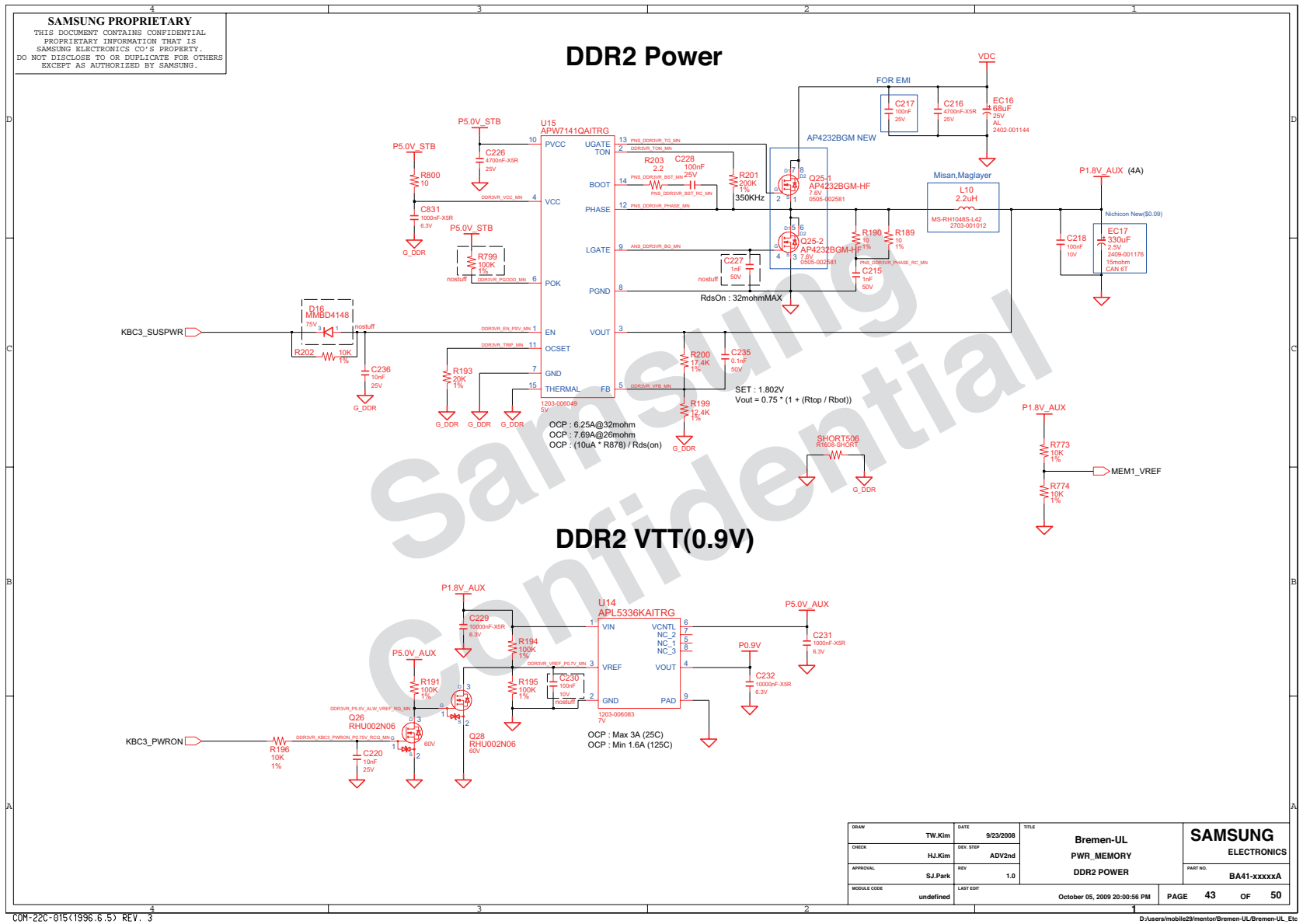


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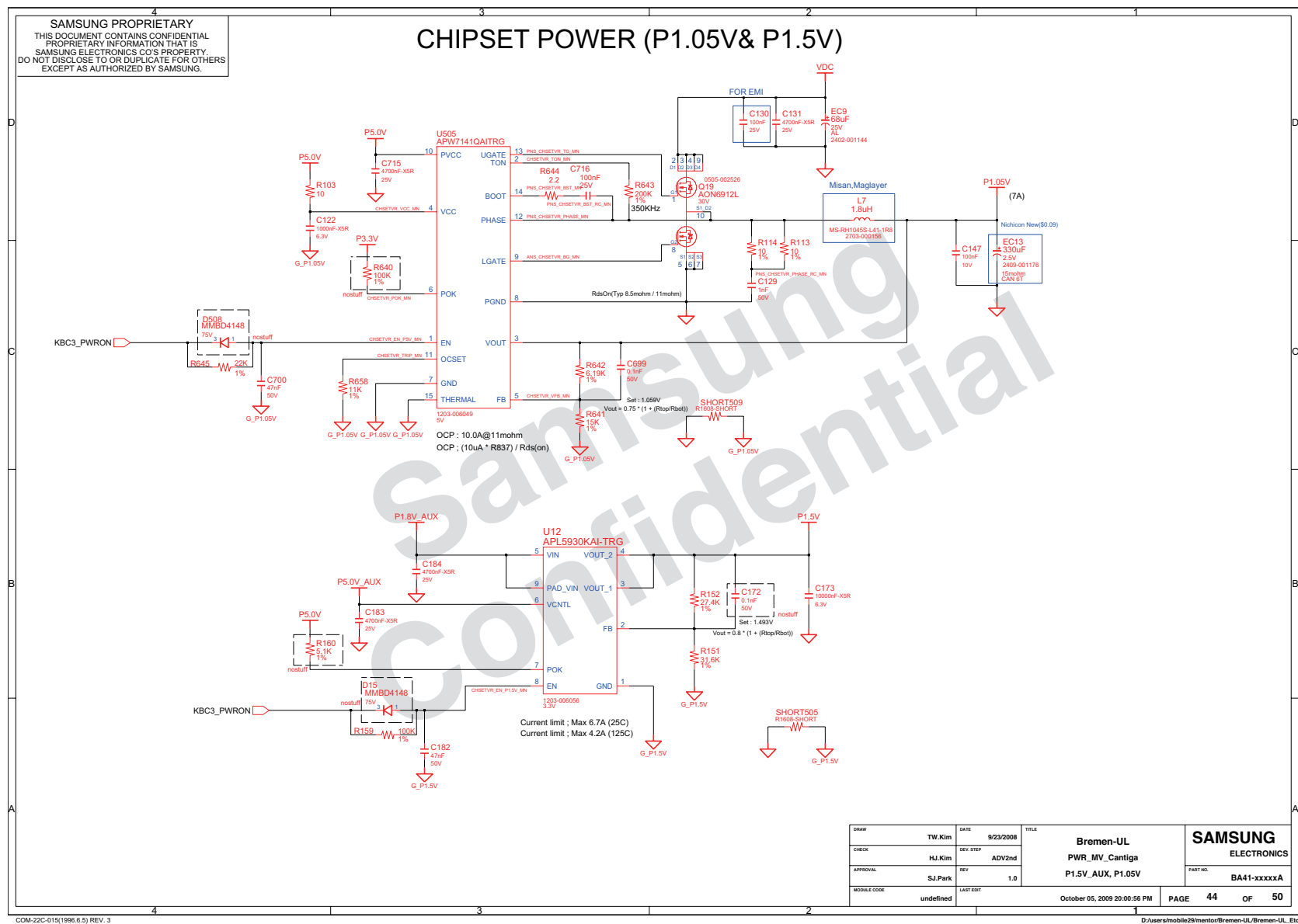




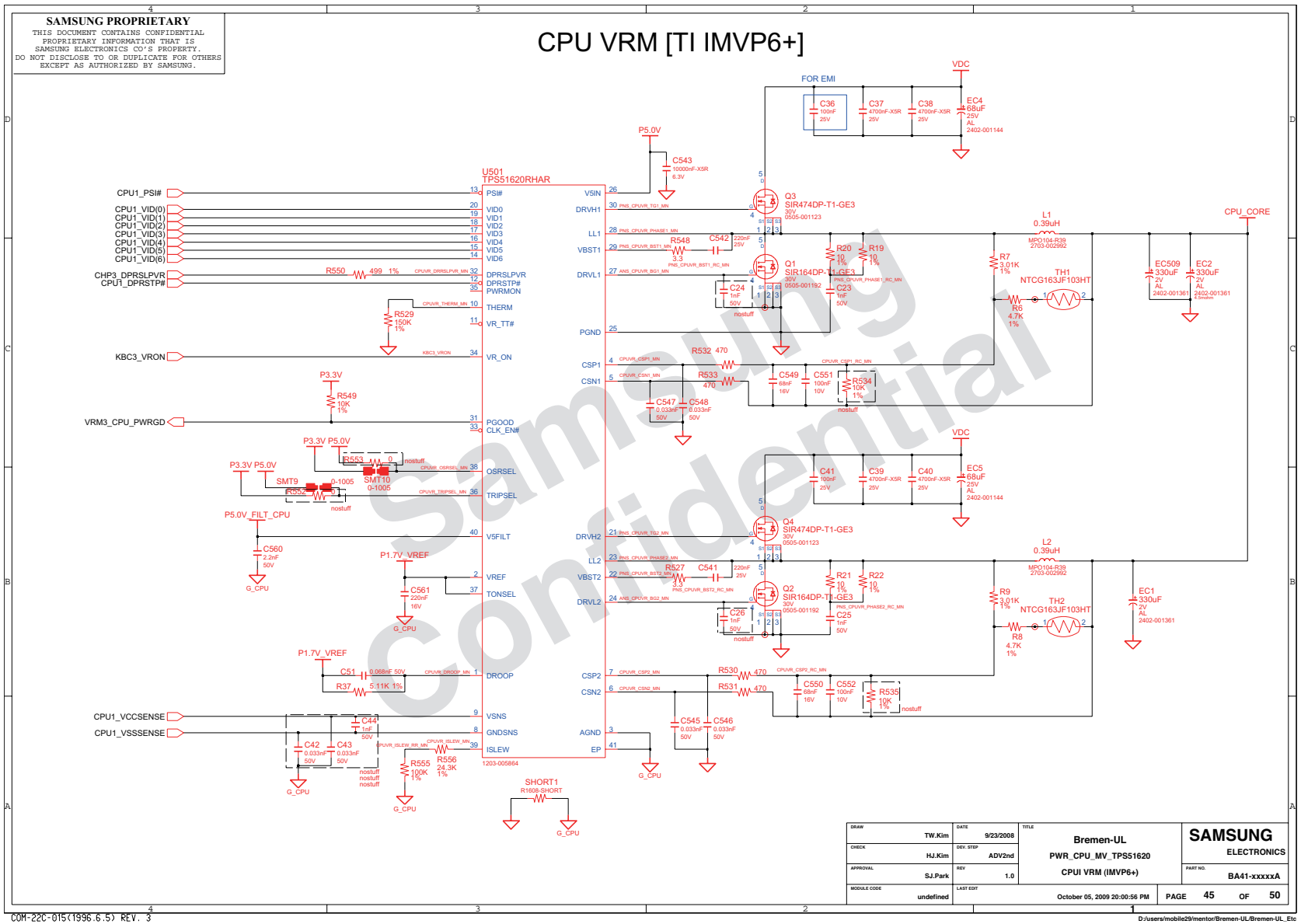
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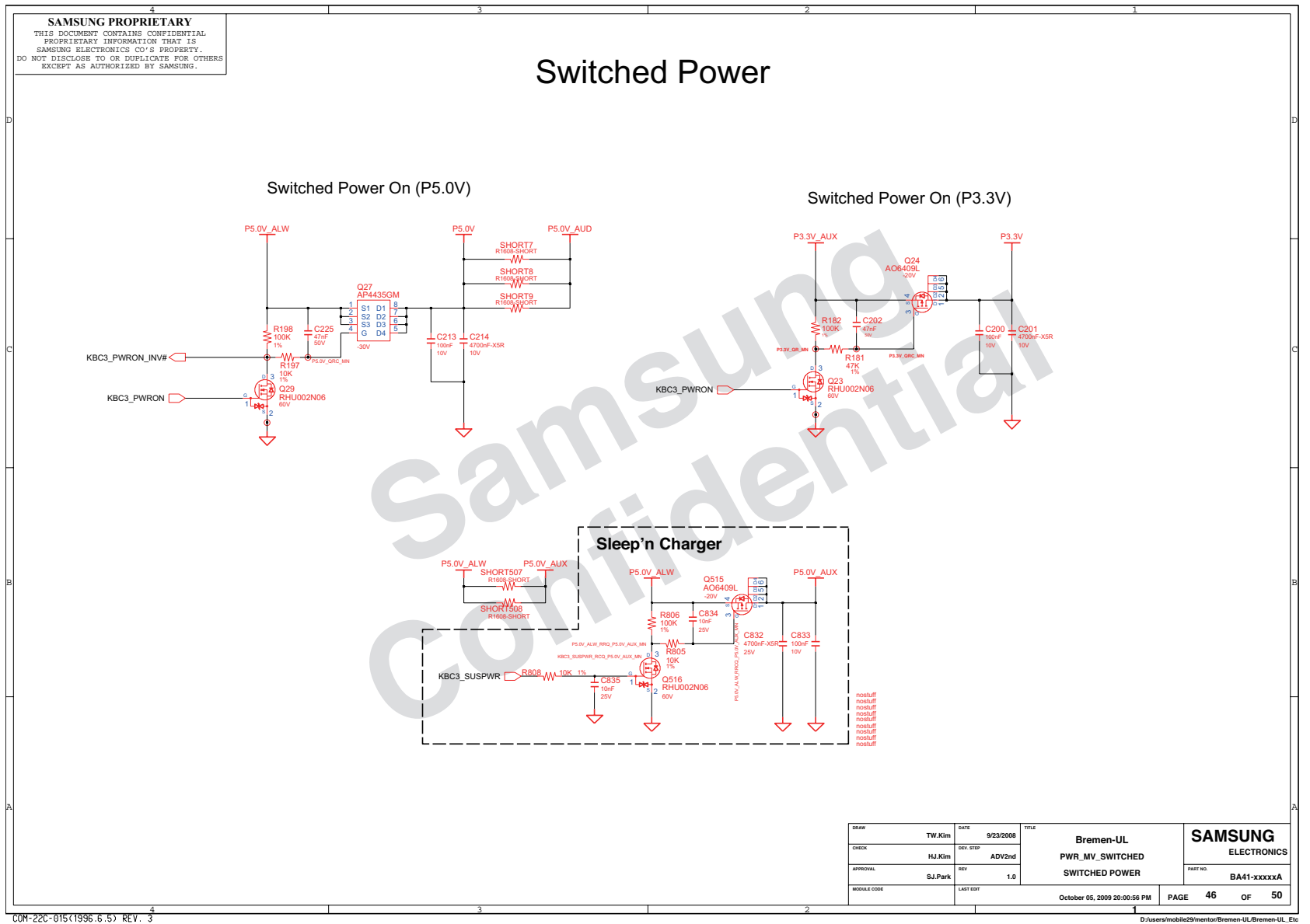
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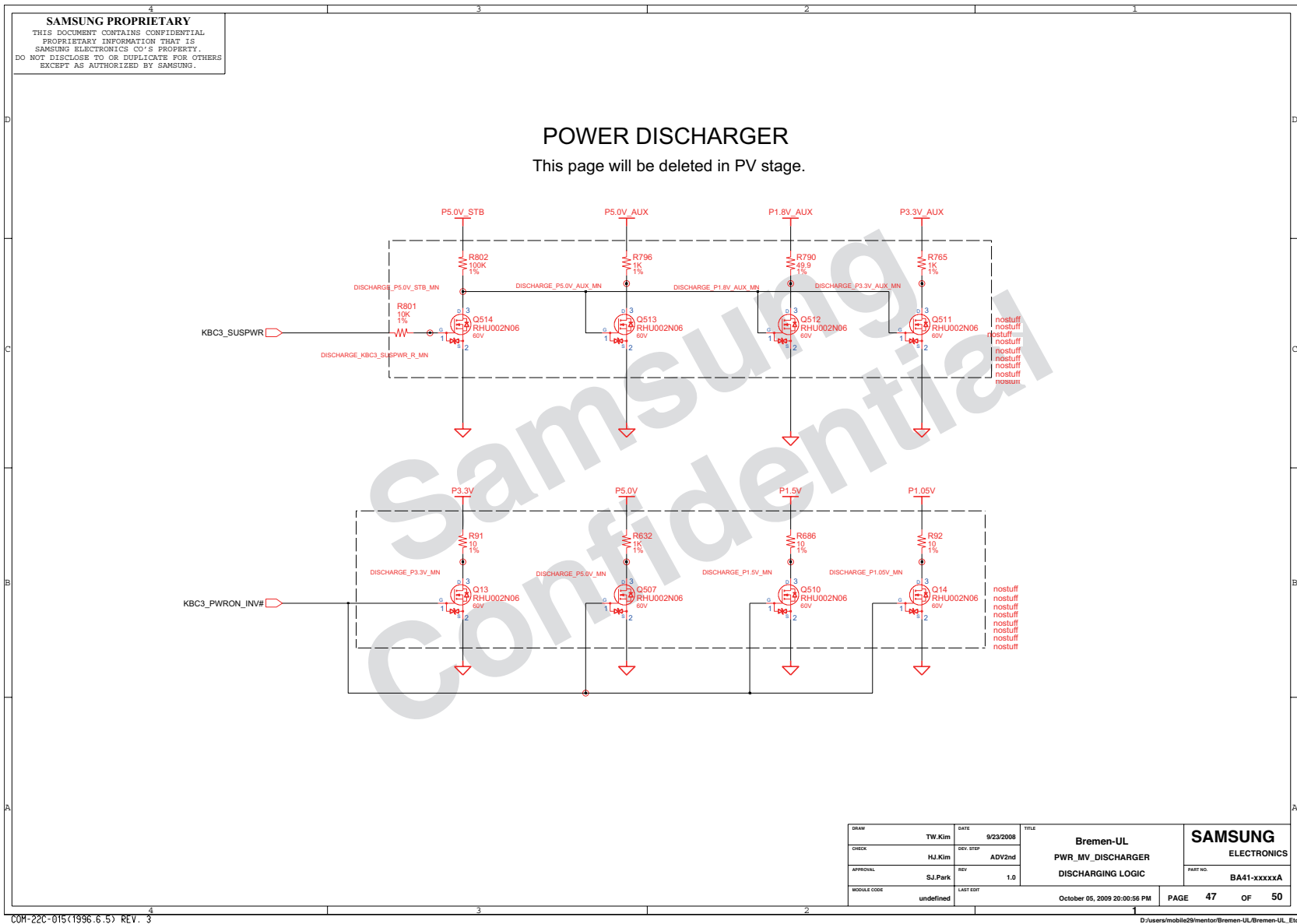
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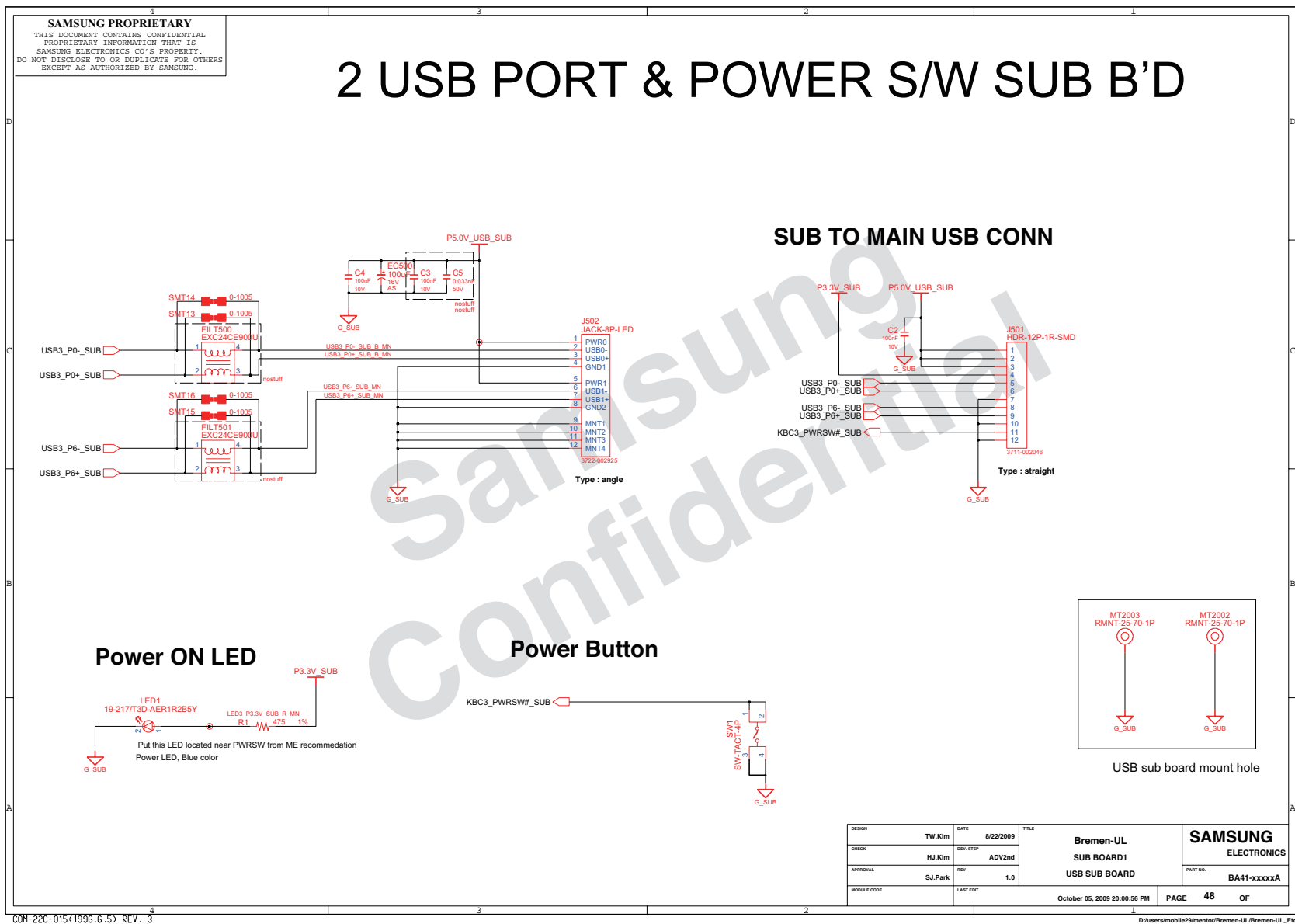
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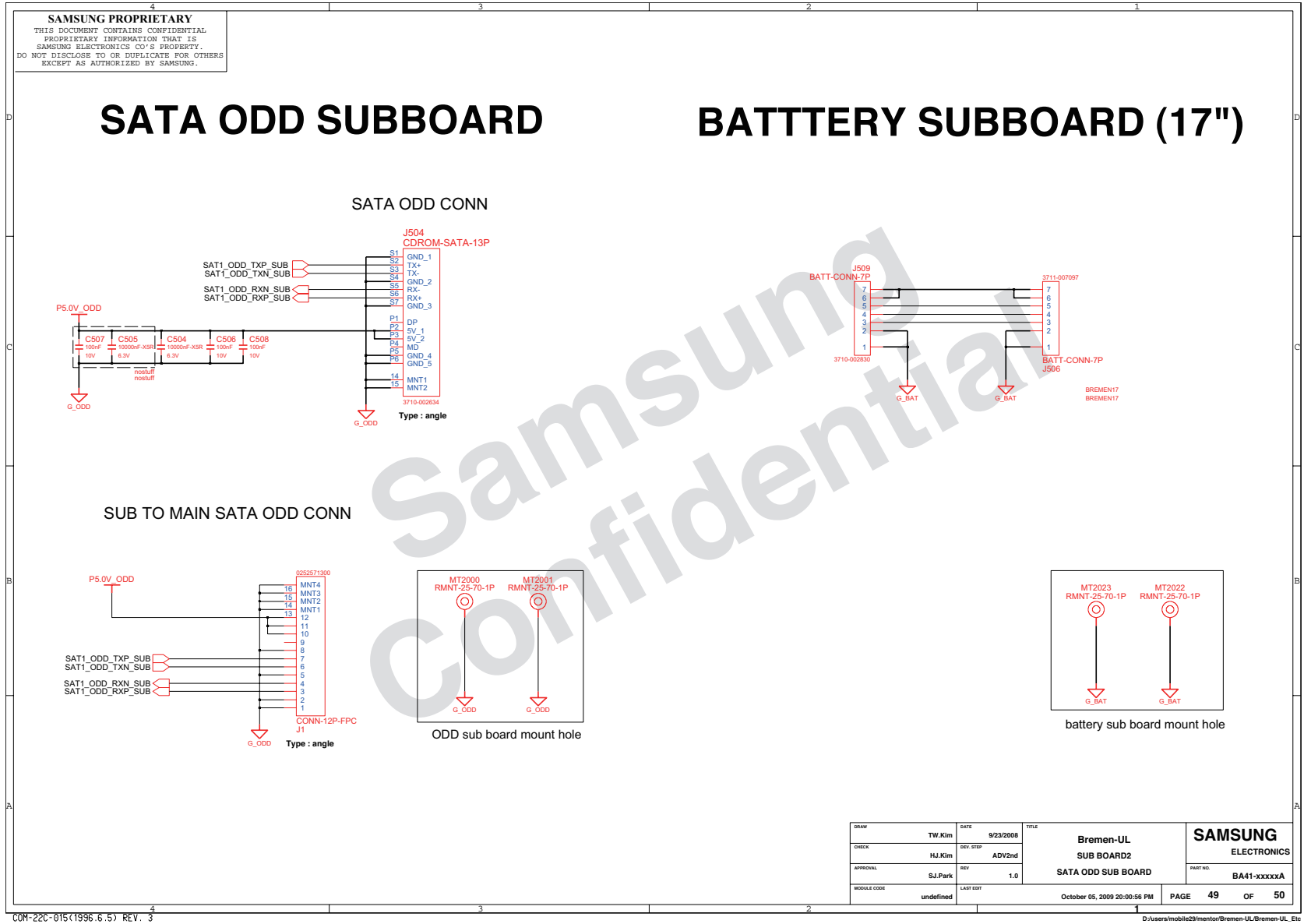
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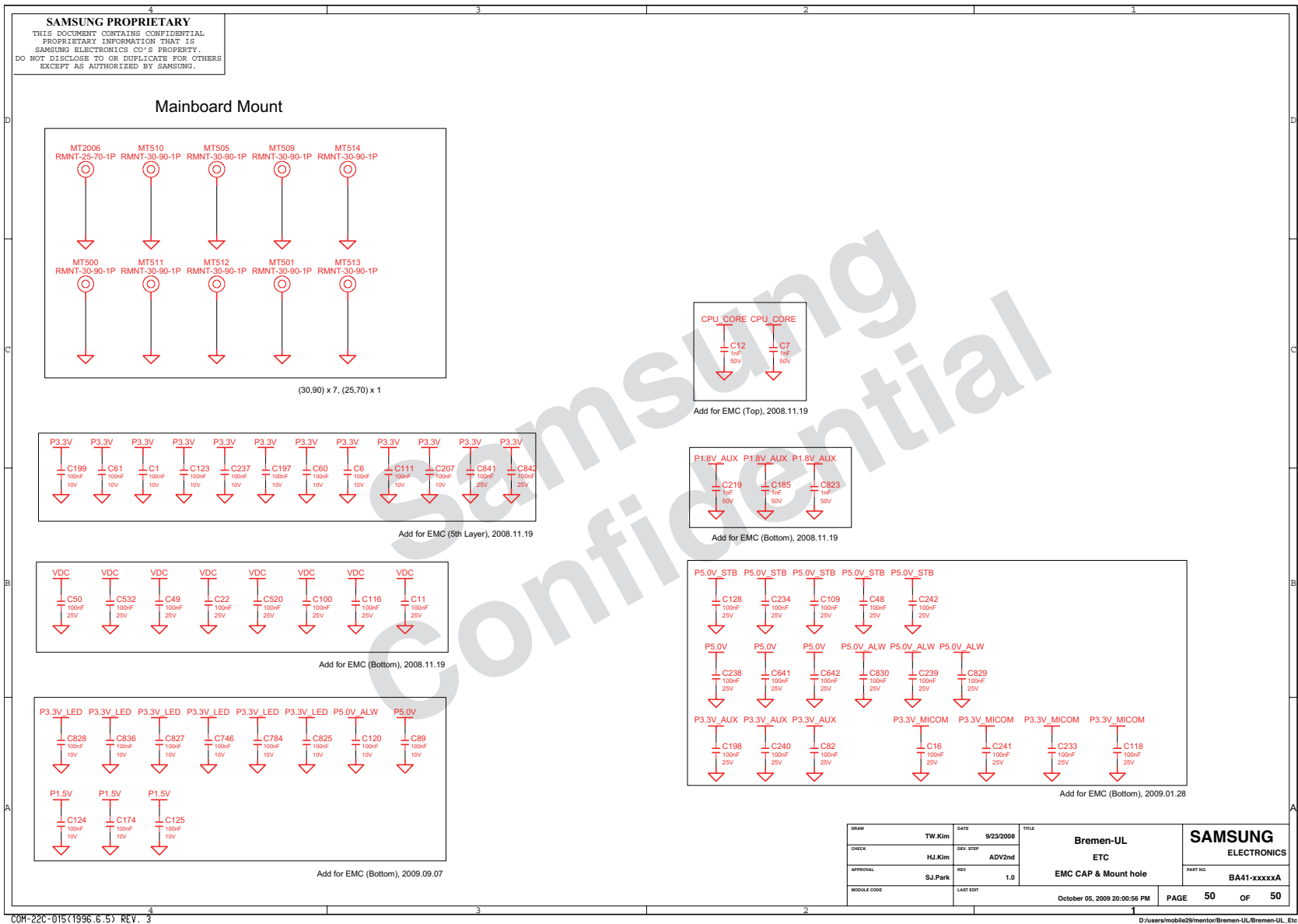
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